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S5102

ERROR RATE TEST SET

TRANSMITTER

INSTRUCTION MANUAL

FORM 0195-0382C

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A UNIT OF GENERAL SIGNAL

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GENERAL SIGNAL

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S5102

ERROR RATE TEST SET

TRANSMITTER

INSTRUCTION MANUAL

FORM 0195-0382C

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Phone (617)256-9013 Telex 951952

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SECTION 1
INTRODUCTION

GENERAL DESCRIPTION

This manual provides the information required to install, operate, and maintain the Model S5102 Error Rate Test Set Transmitter (hereinafter referred to as the "Transmitter Test Set" or the "Test Set").

The Transmitter Test Set may be used separately or in conjunction with the S5102 Receiver and KS-20775 Error Rate Test Sets which are designed to test T-Carrier communications equipment at standard DS1, DS1C, or DS2 rates utilizing error counting techniques.

The Transmitter Test Set with the MUX ON/OFF pushbutton ON will simulate standard DS1 (1.544 Mb/s), DS1C (3.152 Mb/s), and DS2 (6.312 Mb/s) PCM transmission rates through M1C, M12, and the low speed sections of M13 multiplexers.

The DS1 transmitter output is the Bell System standard $2^{20}-1$ data sequence with 15 zero suppression. The transmitter multiplexes the basic DS1 channel rate to provide a true formatted DS1C and DS2 output with proper framing bits. The DS1C output contains two individual channels of the DS1 data sequence with DS1C framing bits. The DS2 output contains four individual channels of the DS1 data sequence with DS2 framing bits.

When the MUX ON/OFF pushbutton is OFF, the transmitted data sequence at each DS rate will be a standard $2^{20}-1$ pseudorandom pattern. During this mode of operation neither multiplexing nor framing bits are added to the data pattern.

Physical Description

The transmitter is contained in a 9¼" (H) x 13" (W) x 11-3/4" (D) enclosure that weighs approximately 16 lbs (refer to fig. 1-1). All major controls and indicators required to operate the Test Set are located on the front panel and described in Section 3. Auxiliary connectors are provided on the rear of the unit and are used as signal sources for testing purposes in conjunction with the S5102 error rate test set (receiver).

The Test Set requires only the application of 115 VAC, 60 Hz power through a 3/4A slow blow fuse (F1) on the front panel. Power is applied to the front panel through the use of the power cable supplied with the Test Set.

The DC power supply that supplies the required voltages to the printed circuit boards is mounted in the Test Set, as shown in Figure 1-1. A detailed description of the power supply is provided in Appendix A. DC power distribution to the PC boards is provided through the printed circuit backplane that interconnects the printed circuit boards.

The Test Set meets or exceeds all Bell System Test Set design requirements, including rounded edges on all outer surfaces, panel designations that can be easily read under low level light conditions, permanent operational instructions applied to the outer surface of the enclosure, guard handles to protect front-panel controls and indicators, rubber feet on bottom and back of the Test Set, and detachable cover and power cord.

Solid-state and discrete components are employed throughout the transmitter with extensive use of integrated circuits for extended reliability. Printed circuit boards are connected into the system by a printed circuit backplane mounted on the bottom of the Test Set. Interconnection from the circuit boards to the front panel are point-to-point wired.

THE LOCATION OF MAJOR COMPONENTS IN THE TEST SET ARE LISTED IN FIG. 1-1 AND DEFINED IN TABLE 1-1.

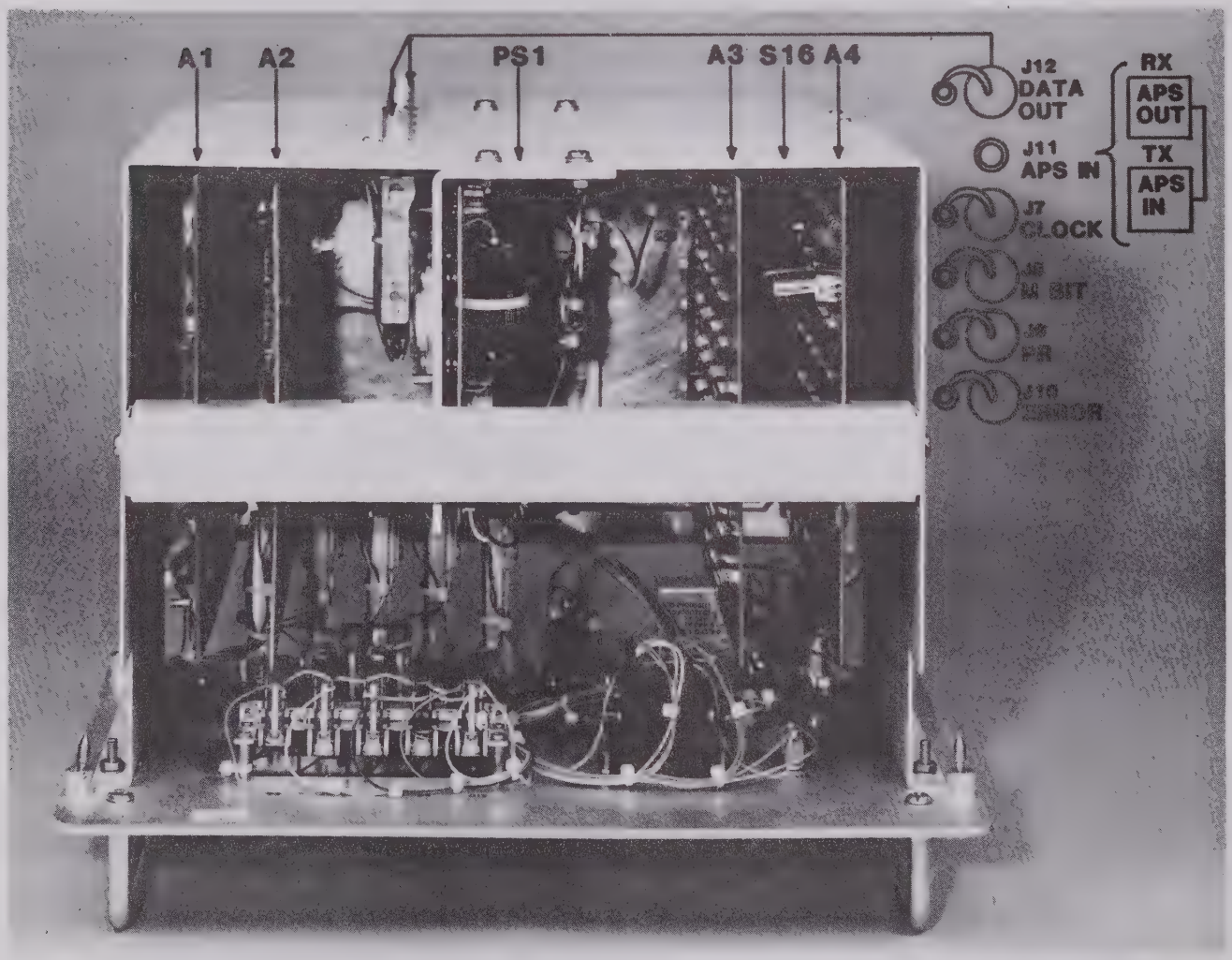

FIGURE 1-1 TRANSMITTER TEST SET MAJOR COMPONENTS (TOP VIEW, ENCLOSURE REMOVED)

TABLE 1-1
MAJOR COMPONETS

INDEX NUMBER	COMPONENTS (REFER TO FIG. 1-1)
A1	OUTPUT AMPLIFIER PRINTED CIRCUIT BOARD (PC5).
A2	ENCODER AND ERROR CONTROL PRINTED CIRCUIT BOARD PC4).
A3	MULTIPLEXER CONTROL PRINTED CIRCUIT BOARD (PC3).
A4	PATTERN GENERATOR PRINTED CIRCUIT BOARD (PC2).
PS1	DC POWER SUPPLY (REFER TO APPENDIX A).
S16	TEST/NORMAL SLIDE SWITCH, FOR DISPLAYING ALL-ONES DATA.
J7	CLOCK OUT CONNECTOR, DEPENDIENT UPON SELECTED RATE.
J8	M-BIT OUTPUT CONNECTOR, FOR TEST PURPOSES.
J9	PR PSEUDORANDOM SIGNAL FRAME OUTPUT CONNECTOR, FOR TEST PURPOSES.
J10	ERRORS BIPOLAR VIOLATION OR BIT ERROR OUTPUT CONNECTOR, FOR TEST PURPOSES.
J11	APS IN WECO 310-TYPE CONNECTOR FOR AUTOMATIC PROTECTION SWITCHING SIGNAL.
J12	DATA OUT CONNECTOR, DEPENDENT UPON SELECTED RATE.

FUNCTIONAL DESCRIPTION

THE TEST SET GENERATES DATA AND CLOCK SIGNALS WHICH SIMULATE THE OUTPUT OF BELL-COMPATIBLE T-CARRIER COMMUNICATIONS LINE EQUIPMENT. THE BASIC TRANSMITTER DATA OUTPUT IS A $2^{20}-1$ MAXIMUM LENGTH PSEUDORANDOM SEQUENCE AT THE DS1 RATE WITH FIFTEEN (15) ZERO SUPPRESSION AND ALTERNATE MARK INVERSION (AMI) CODING.

THIS DS1 PATTERN IS ALSO THE BASIS FOR THE DS1C RATE WHERE A

DELAYED AND INVERTED DS1 PATTERN IS MULTIPLEXED WITH THE BASIC PATTERN. THIS COMPOSITE IS THEN SCRAMBLED BY A MODULO-2 ADDER AND COMBINED WITH DS1C HOUSEKEEPING AND STUFFING BITS AND AMI CODED TO FORM THE DS1C OUTPUT.

THE DS2 RATE IS DERIVED IN THE SAME MANNER. HOWEVER, ONLY THE DS1 PATTERN AND THE DELAYED, INVERTED DS1 PATTERN ARE DUPLICATED. THE BASIC PATTERNS (DS1) AND THE 3 DELAYED VERSIONS (2 BEING INVERTED) ARE MULTIPLEXED. UNLIKE THE DS1/DS1C RATE, HOWEVER, THE DS2 IS DIRECTLY COMBINED WITH THE DS2 HOUSEKEEPING AND STUFFING BITS AND ENCODED WITH THE B6ZS CODE. THIS SIGNAL IS THEN ATTENUATED AND SHAPED WITH NETWORKS FOR HI, LO, AND DSX LEVELS THAT ARE REQUIRED TO TEST VARIOUS TERMINALS AND LINE EQUIPMENT.

IN ADDITION TO THE STANDARD PSEUDORANDOM DATA OUTPUT, SINGLE BIT ERRORS AND VARIABLE RATES OF BIPOLAR VIOLATIONS CAN BE INSERTED IN THE DS OUTPUT SIGNALS. A FRONT-PANEL CONTROL ALSO ALLOWS THE SELECTION OF AN ALL ONE'S DATA OUTPUT AT THE DS1 RATE MULTIPLIED UP TO THE DS1C OR DS2 RATE IN THE NORMAL MANNER. IN DS1C/DS2 RATES, NORMAL MULTIPLEXER OPERATION IS IN EFFECT. AN INTERNAL SWITCH IS AVAILABLE TO PROVIDE AN ALL ONE'S OUTPUT WITHOUT FRAMING AND CONTROL BITS.

OPERATING REQUIREMENTS

THE FOLLOWING PARAGRAPHS BRIEFLY COVER THE OPERATING REQUIREMENTS FOR THE TRANSMITTER TEST SET. ALL GENERAL REQUIREMENTS THAT ARE NORMALLY ASSOCIATED WITH ELECTRONIC EQUIPMENT WILL APPLY TO THIS UNIT.

Personnel Requirements

The Test Set may be efficiently operated and adequately maintained by personnel skilled in electronic technology and digital logic circuitry. They should also be familiar with the required communications equipment with which the Test Set is designed to interface.

Environmental Requirements

For most efficient operation, the following conditions are recommended:

- Ambient temperature between 0^{o} C and 50^{o} C.
- Relative humidity of 10% to 95% (non-condensing).

Equipment Required But Not Supplied

Normal operation of the Test Set requires cables for interconnecting the Test Set to the communications equipment with which it will be operated. Section 2 of this manual provides a description of the required cables and their part numbers. Table 5-1 in Section 5 lists the test equipment required for maintenance.

WARRANTY

All Tau-Tron products are warranted against any defects in material and workmanship. This warranty applies for one year from the date of delivery for all Tau-Tron manufactured products. The warranty period for OEM products sold by

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FOR ANY ASSISTANCE, CONTACT THE FACTORY AND BE PREPARED TO PROVIDE INSTRUMENT MODEL AND SERIAL NUMBERS AND ALL DETAILS REGARDING THE MALFUNCTION.

SECTION 2
INSTALLATION

INTRODUCTION

This section provides the information necessary to unpack and test the S5102 Transmitter Test Set for normal operation.

UNPACKING INSTRUCTIONS

The Test Set is shipped in a corrugated container that has been lined with bubblewrap and sealed with pressure sensitive tape. Carefully cut the tape sealing the container and remove the protective material with the Test Set as a whole. Strip off the bubblewrap.

CABLE REQUIREMENTS

The 115 VAC input power cable that is connected to the front panel of the Test Set is the only cable supplied with the Test Set. The other cable requirements to operate the Test Set are those terminated in the WECO 310 compatible plugs and the BNC type monitor plugs that connect the front and rear of the Test Set. Refer to Table 2-1.

Reference Designation	QTY	Location	Connector Plug And Function
DS1/DS1C	4	Front Panel	WECO 310 (or equivalent connected to a 110 ohm balanced twisted pair shielded cable for transmitted output, (refer to Table 3-1 for functional definition of test set connector).
DS2	1	Front Panel	
APS (J11)	1	Rear Panel	
DATA OUT (J12)	1	Rear Panel	BNC connector (or equivalent) connected to a 75 ohm coaxial cable to monitor internal test set signals. (Refer to Table 3-1 for function definition of Test Set connector).
Clock (J7)	1	Rear Panel	
M BIT (J8)	1	Rear Panel	
PR (J9)	1	Rear Panel	
ERROR (J10)	1	Rear Panel	
TEST/NORMAL (J16)	1	Rear Panel	Slide switch kept in normal position for test set purposes. If put in test position, all-ones DATA are displayed.

NOTE: The twisted pair shielded cable connected to the WECO 310 connector MUST be balanced at 110 ohms to produce optimum output, (ADC Products, PJ-8, series, WECO P3BH, or equivalent).

SECTION 3
OPERATING INSTRUCTIONS

INTRODUCTION

The operating instructions for the Test Set are described in the following paragraphs by first defining the functions of all the controls and indicators that are on the front panel (Table 3-1) and cross-referencing each function to its specific physical location in Figure 3-1.

Once the operator is familiar with the location and function of the controls and indicators, the operational procedures are described. This includes initial turn-on procedures, test set operating procedures for DS1, DS1C, and DS2 rates, a self test, and normal shutdown of the equipment.

CONTROLS AND INDICATORS

The controls and indicators for the Test Set are listed in Table 3-1 according to the nomenclature on the front panel (e.g., REDUCE TEST LEVEL, SINGLE BIT ERROR, etc.) These definitions are further grouped into subdivisions on the panel, i.e., OUTPUTS, TEST, and BIPOLAR VIOLATION INSERTION. Table 3-1 is also cross-referenced according to the INDEX NUMBER column with that of Figure 3-1 in an effort to familiarize the operator with the controls and indicators in the shortest possible time. Throughout this manual, reference to specific controls and indicators will be written as they appear on the front panel of the Test Set.

TABLE 3-1
TRANSMITTER TEST SET OPERATING CONTROLS AND INDICATORS

INDEX NUMBER	CONTROL OR INDICATOR	FUNCTION
1	KX10-N/APS CONTROL	SELECTS BIPOLAR VIOLATION RATES TO BE INJECTED INTO THE DATA STREAM THROUGH A RANGE OF 1x10-8 TO 9x10-3. USED TO CHECK T-CARRIER AUTOMATIC PROTECTION SWITCHES.
2	CONTINUOUS/OFF MOMENTARY TOGGLE SWITCH	SELECTS THE MODE THAT IS EMPLOYED TO INJECT BIPOLAR VIOLATIONS.
3	REDUCE TEST LEVEL PUSHBUTTON	REDUCES THE AMPLITUDE OF THE OUTPUT SIGNAL. DS1 - 24 DB IN SERIES WITH DSX OUTPUT. DS1C - 24 DB IN SERIES WITH DSX OUTPUT. DS2 - 40 DB ADDED IN SERIES WITH THE HI, DSX, AND LO OUTPUTS.
4	SINGLE BIT ERROR PUSHBUTTON	A SINGLE BIT ERROR IS INJECTED INTO THE PSEUDORANDOM DATA PATTERNS OF EACH DS1 CHANNEL EACH TIME THIS BUTTON IS PUSHED IN.
5	"X" BIT DS1C/2 PUSHBUTTON.	CHANGES THE X-BIT LOGIC STATE. (CHANGES A LOGIC ONE TO A ZERO) AT DS1C AND DS2 RATES WHILE THE BUTTON IS PUSHED IN.
6	POWER LOST INDICATOR	INDICATES THAT POWER WAS LOST FOR AN INTERVAL OF TIME. IT IS RESET BY THE RESET PUSHBUTTON.
7	RESET PUSHBUTTON	RESETS THE POWER LOST INDICATOR.
8	POWER PUSHBUTTON INDICATOR	APPLIES POWER TO THE TEST SET.
9	DS2 OUTPUT JACK (J5)	PSEUDORANDOM OR ALL ONE'S TRANSMITTED OUTPUT, DEPENDENT ON SELECTION OF DATA SWITCHES, AND REQUIRES DS2 (HI, DSX, OR LO) SELECTION. THIS OUTPUT CONTAINS FOUR DS1 CHANNELS THAT HAVE BEEN MULTIPLEXED AND INCLUDES FRAMING AND CONTROL BITS THAT ARE BELL-COMPATIBLE.
10	DS1/DS1C OUTPUT JACKS (J1 - J4)	PSEUDORANDOM OR ALL ONE'S TRANSMITTED OUTPUT, DEPENDENT ON SELECTION OF DATA SWITCHES AND DS1, OR DS1C OUTPUT. THE DS1C OUTPUT CONTAINS TWO DS1 CHANNELS THAT HAVE BEEN MULTIPLEXED AND INCLUDES FRAMING AND CONTROL BITS THAT ARE BELL-COMPATIBLE.
11	DATA/PR CONTROL	SELECTS A PSEUDORANDOM OUTPUT (2^{20}-1) 1,048,575 WORD, SELF-STARTING, 15 ZERO SUPPRESSION.
12	DATA/ONE'S CONTROL	SELECTS A BIT STREAM OUTPUT OF LOGICAL ONE'S.
13	MUX ON/OFF	SELECTS FRAMED (ON) OR UNFRAMED (OFF) FORMAT.
14	DS1/DSX CONTROL	SELECTS TRANSMITTER OUTPUT AT THE 1.544 MB/S RATE AND DSX LEVEL.
15	DS1C/DSX CONTROL	SELECTS TRANSMITTER OUTPUT AT THE 3.152 MB/S RATE AND DSX LEVEL.
16	DS2/HI CONTROL	SELECTS TRANSMITTER OUTPUT AT THE 6.312 MB/S RATE AND HI AMPLITUDE.
17	DS2/DSX	SELECTS TRANSMITTER OUTPUT AT THE 6.312 MB/S RATE AT THE DSX AMPLITUDE. (SERIES LOAD OF 1000 FEET ABAM CABLE, SIMULATED).
18	DS2/LO CONTROL	SELECTS TRANSMITTER OUTPUT AT 6.312 MB/S AND LO AMPLITUDE (6 DB IN SERIES WITH 2000 FEET OF ABAM CABLE, SIMULATED).

NOTE: MONITOR SIGNALS THAT ARE BROUGHT-OUT TO CONNECTORS ON THE REAR PANEL ARE DESCRIBED IN TABLE 1-1.

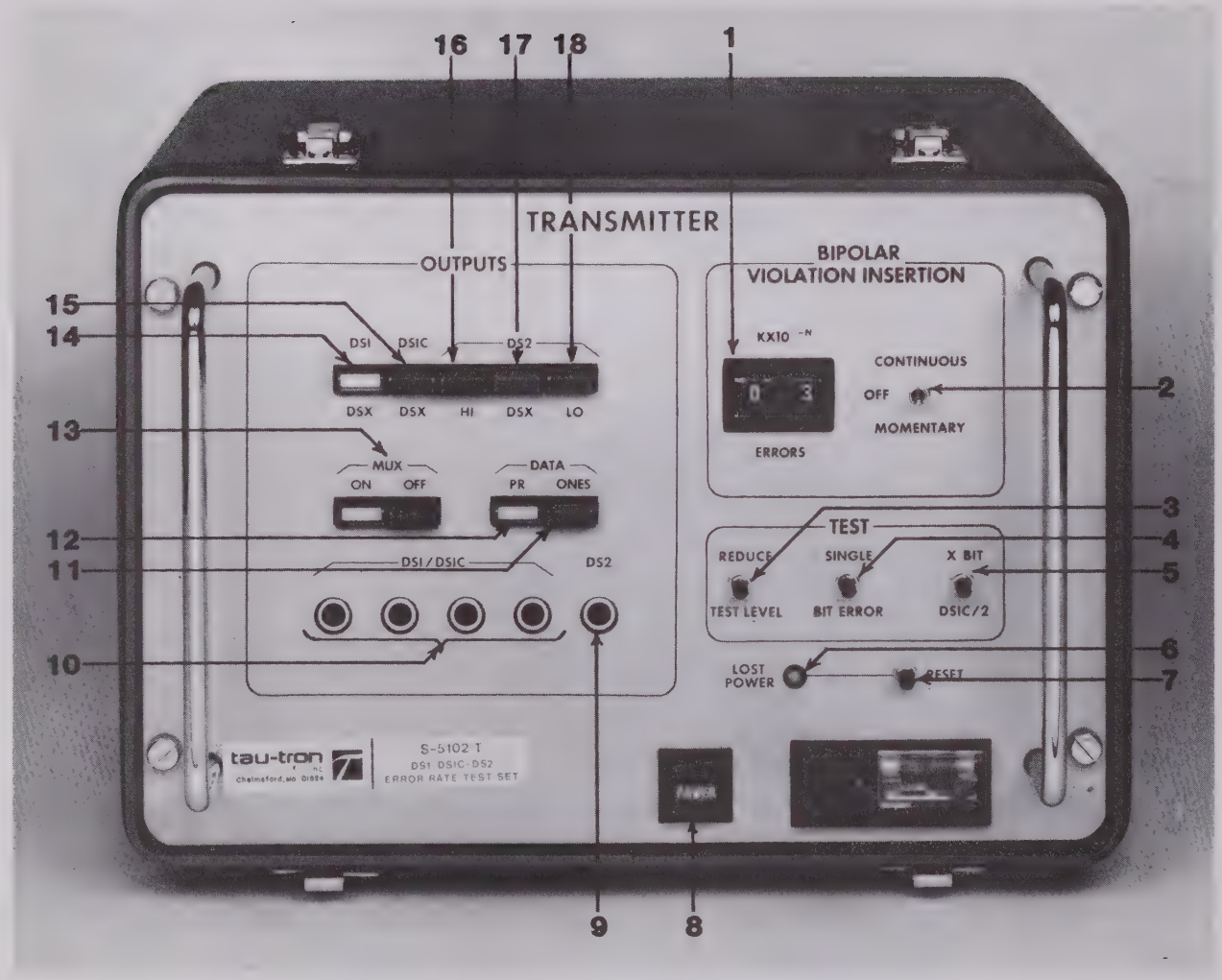


FIGURE 3-1 TRANSMITTER TEST SET OPERATING CONTROLS AND INDICATORS.

TURN-ON PROCEDURE

THE ONLY EXTERNAL POWER REQUIREMENT FOR THE TEST SET IS THE POWER CABLE THAT IS PLUGGED INTO THE RECEPTACLE ON THE FRONT PANEL OF THE TEST SET AND TO A SOURCE OF 115V ± 10%, 55 TO 65 HZ. THE TRANSMITTER IS TURNED ON BY PUSHING IN THE POWER PUSHBUTTON/INDICATOR ON THE FRONT PANEL (SEE TABLE 3-1).

OPERATION (REFER TO FIGURE 3-1)

SELECT THE APPROPRIATE DS RATE (DS1, DS1C, OR DS2) AND/OR OUTPUT LEVEL WITH THE MUX ON/OFF PUSHBUTTON ON. DS2 REQUIRES A HI, DSX, OR LO SELECTION ON THE FRONT PANEL. THIS IS FOLLOWED BY THE SELECTION OF A DATA PATTERN OF EITHER PR OR ONES. ONE OR MORE OF THE FOUR OUTPUT JACKS FOR THE DS1/DS1C OR THE SINGLE OUTPUT JACK (ALL WECO 310 COMPATIBLE) FOR DS2 IS THEN USED TO INTERCONNECT THE TEST SET AND THE COMMUNICATIONS EQUIPMENT UNDER TEST.

BIPOLAR VIOLATIONS MAY BE INSERTED USING THE $KX10^{-N}$ THUMBWHEEL SWITCH, WHERE K SELECTS THE INTEGER (1-9) AND N SELECTS THE EXPONENT (3-8). THE CONTINUOUS/OFF/MOMENTARY TOGGLE SWITCH ACTIVATES THE VIOLATION CONTINUOUSLY OR MOMENTARILY (CENTER POSITION IS OFF).

PUSHING IN THE "X" PUSHBUTTON AT EITHER THE DS1C OR DS2 RATE WILL CHANGE THE TRANSMITTED X-BIT (ALARM SERVICE BIT) FROM ITS NORMAL ONE VALUE TO A ZERO. WHEN THE SWITCH IS RELEASED, THE TRANSMITTED BIT RETURNS TO ITS NORMAL LOGIC LEVEL.

THE SINGLE BIT ERROR PUSHBUTTON INJECTS A LOGIC BIT ERROR INTO THE PSEUDORANDOM TEST SEQUENCE. THIS ERROR WILL APPEAR IN EACH DS1 CHANNEL COMPRISING THE FINAL OUTPUT SIGNAL. SPECIFICALLY, AN ERROR WILL APPEAR IN BOTH DS1 CHANNELS OF A DS1C SIGNAL AND ALL FOUR CHANNELS OF A DS2 SIGNAL.

THE REDUCE TEST LEVEL PUSHBUTTON REDUCES THE TEST LEVEL AMPLITUDE BY 24 dB IN DS1, 24 dB IN DS1C, AND 40 IN DS2. WHEN POWER IS INITIALLY APPLIED TO THE TEST SET, OR WHEN POWER TO THE TEST SET HAS BEEN MOMENTARILY LOST, THE LOST POWER LAMP WILL BE ILLUMINATED AND CAN BE RESET BY THE RESET PUSHBUTTON.

THE TEST SET CAN ALSO BE USED TO TEST THE AUTOMATIC PROTECTION SWITCH (APS) OPERATION IN CONJUNCTION WITH A COMPATIBLE RECEIVER TEST SET S5102. DATA THAT ARE RECEIVED AT THE INPUT CONNECTOR OF THE RECEIVER TEST SET ALSO APPEAR AT THE APS OUT CONNECTOR ON THE REAR OF THE RECEIVER TEST SET. THE DATA FROM THIS CONNECTOR CAN BE COUPLED TO THE APS IN CONNECTOR AT THE REAR OF THE TRANSMITTER TEST SET, WHICH ROUTES DATA INTO A CIRCUIT THAT INSERTS BIPOLAR VIOLATIONS INTO THE OUTPUT AMPLIFIERS FOR RE-TRANSMISSION THROUGH THE COMMUNICATIONS EQUIPMENT TO THE RECEIVER TEST SET. (REFER TO FIG. 3-2).

NOTE: USE WITH SYSTEM SIGNALS (COMMANDS TO REMOTE SWITCHES), SET CAN BE USED TO TEST MARGINS WITHOUT APS CONNECTOR.

BIPOLAR VIOLATIONS CAN THEN BE INSERTED ONTO THE DATA AT VARIOUS RATES IN ORDER TO CHECK THE TRIP, HOLD, AND RESET POINTS OF THE SWITCH.

FIGURE 3-2 APS CONNECTION

SHUTDOWN PROCEDURE

THE TEST SET TRANSMITTER REQUIRES NO SPECIFIC SHUTDOWN PROCEDURE. ONCE THE INPUT SIGNAL PLUG HAS BEEN REMOVED, THE POWER PUSHBUTTON INDICATOR MAY BE PUSHED, THE POWER PLUG REMOVED, AND THE TEST SET COVER REPLACED.

SECTION 4
PRINCIPLES OF OPERATION

INTRODUCTION

This section contains the theory of operation for the S5102 Error Rate Test Set (Transmitter) and is discussed at two levels. The first level is an overall description based on the functuonal block diagram (Fig. 6-1). The second is based on the schematic and component location diagrams (Figs. 6-2 through Figs. 6-8). The transmitter specifications are listed in Table 4-1.

OVERALL FUNCTIONAL DESCRIPTION

The four major functional areas of the Transmitter Test Set are illustrated in Fig. 6-1 and the general theory of operation is described in the following paragraphs.

Pattern Generator

The pattern generator board generates the three DS rate clock signals (1.544 MHz, 3.152 MHz, and 6.312 MHz), the basic pseudorandom test sequence, and the required M,F,X, and C control bits.

TABLE 4-1
TRANSMITTER SPECIFICATIONS

	DS1	DS1C	DS2
CLOCK			
FREQUENCY	1.544 MHz	3.152 MHz	6.312 MHz
STABLILITY	TEMPERATURE: 0 TO +50° C., ±10 PPM AGING RATE PER MONTH, ±1 PPM		
OUTPUT			
COMPOSITION			
MUX ON	ONE DS1 CHANNEL UNFRAMED 2^{20}-1 PRBS OR ALL-ONES DATA	TWO DS1 CHANNELS FRAMED 2^{20}-1 PRBS OR ALL-ONES DATA INTRODUCED AT DS1	FOUR DS1 CHANNELS FRAMED 2^{20}-1 PRBS OR ALL-ONES DATA INTRODUCED AT DS1
MUX OFF	DS1 RATE UNFRAMED 2^{20}-1 PRBS OR ALL-ONES DATA	DS1C RATE UNFRAMED 2^{20}-1 PRBS OR ALL-ONES DATA	DS2 RATE UNFRAMED 2^{20}-1 PRBS OR ALL-ONES DATA
CODE	AMI	AMI	B6ZS
LEVEL	DSX: ±3.0 V ±0.3 V, SHAPE IS CROSS CONNECT COMPATIBLE.		HIGH:±2.1V ±0.25V DSX: HIGH OUTPUT IN SERIES WITH A 1000 FT. ABAM CABLE SIMULATIOR. LOW: DSX OUTPUT IN SERIES WITH A 1000 FT. ABAM CABLE SIMULATOR AND A 6 DB ATTENUATOR.
REDUCED LEVEL	24 DB OF ATTENUATION IS ADDED IN SERIES WITH NORMAL DSX OUTPUT.		40 DB OF ATTENUATION IS ADDED IN SERIES WITH THE OUTPUT.
INTERFACE	FOUR SEPARATE FRONT-PANEL CONNECTORS (WECO 310 PLUG-COMPATIBLE).		ONE FRONT-PANEL CONNECTOR (WECO 310 PLUG COMPATIBLE).
IMPEDANCE	110 OHMS, BALANCED		
RETURN LOSS	26 DB FOR FREQUENCY RANGE 0.3 TO 6.3 MHZ		
FRAMING	NONE (MUX ON/OFF)	1272 BITS INCLUDING 24 CONTROL BITS BELL-COMPATIBLE. (MUX ON)	1176 BITS INCLUDING 24 CONTROL BITS BELL-COMPATIBLE. (MUX ON)
ERROR INJECTION			
BIT	A SINGLE BIT ERROR IS SIMULTANEOUSLY INJECTED INTO EACH DS1 DATA PATTERN BY FRONT-PANEL PUSHBUTTON.		
BIPOLAR	CODE VIOLATION ERROR INJECTION BY FRONT-PANEL THUMBWHEEL SWITCHES RANGE: $1x10^{-8}$ TO $9x10^{-3}$.		

TABLE 4 - 1

TRANSMITTER SPECIFICATIONS (CONTINUED)

	DS1	DS1C	DS2
AUXILIARY FUNCTIONS			
X-BIT CONTROL (MUX ON)	—	FRONT-PANEL SWITCH CHANGES LOGIC STATE OF X-BIT FROM 1 TO 0.	
AC-POWER INDICATOR	LED INDICATOR OF LOW-LINE OR OUTAGE CONDITION		
APS RECEIVER INPUT	REAR-PANEL (WECO 310 PLUG-COMPATIBLE) INPUT FROM S5102 RECEIVER. CLOCK AND DATA ARE PROVIDED TO FACILITATE THE TESTING OF T-CARRIER SPAN LINE AUTOMATIC PROTECTION SWITCHES.		
DATA OUTPUT	THIS PROVIDES AN NRZ OUTPUT SIGNAL OF 5 ± 0.5V, WITH A SOURCE IMPEDANCE OF 75 OHMS, AT A DS2, DS1C, OR DS2 RATE AS SELECTED BY THE FRONT-PANEL PUSH-BUTTONS. THIS SIGNAL, TOGETHER WITH THE REAR-PANEL CLOCK OUTPUT, CAN BE USED IN SITUATIONS WHERE ACCESS TO THE BIPOLAR SIGNAL IS NOT AVAILABLE, OR FOR TROUBLE-SHOOTING A SYSTEM'S INTERNAL CIRCUITRY.		
MONITOR JACKS			
INTERNAL CLOCK	TRANSMISSION RATE		
M-FRAME SYNC (MUX ON)	ONE PER M-FRAME		
PR-FRAME	ONE PER DS1 WORD SEQUENCE		
ERROR INSERT	ONCE PER INSERT LOCATION		
GENERAL			
POWER	115 VAC ± 10%, 50 TO 500Hz, < 40VA		
SIZE	9.25H x 13.0W x 11.75D		
WEIGHT	16 LBS. (7.3 KG)		
ACCESSORIES	POWER CABLE, INSTRUCTION MANUAL, PROTECTIVE COVER.		

MULTIPLEXER CONTROL

THE MULTIPLEXER CONTROL BOARD PROVIDES TWO DISTINCT LOGIC FUNCTIONS. FIRST, IT CONVERTS THE INCOMING DS CLOCK SIGNAL INTO A GAPPED CLOCK WHICH IS USED BY THE PATTERN GENERATOR TO CONTROL THE PSEUDORANDOM SEQUENCE LOGIC. THEN, IT TAKES THE SINGLE DATA INPUT FROM THE PATTERN GENERATOR AND CONVERTS IT INTO THE REQUIRED MULTIPLE DATA TEST PATTERNS WHICH ARE MULTIPLEXED TOGETHER WITH THE APPROPRIATE FRAMING AND CONTROL BITS.

Encoder and Error Control

The Encoder and Error Control board encodes the Non-Return-To-Zero (NRZ) data output from the Multiplexer Control board into a Return-to Zero (RZ) format of positive (P) and negative (N) rails.

These rails drive the output amplifier, forming the bipolar signal. The P and N rails are encoded as Alternate Mark Inversion (AMI) for DS1/DS1C and as Bipolar 6 Zero Substitution (B6ZS) for DS2. This B6ZS is a line code that replaces each occurence of six zeros with the code 0VB0VB where 0 is the absence of a pulse, V is a violation, and B is a normal bipolar pulse. A violation is a pulse whose polarity is the same as the last pulse that was transmitted. Whereas, a normal pulse is one in which its polarity is opposite to that of the last pulse transmitted. The other section of this board is the error control logic which inserts bipolar violations into the data stream. These bipolar violations are controlled by the front-panel thumbwheel switches labeled $K \times 10^{-N}$.

Output Amplifier

The output amplifier board contains four DS1/DS1C amplifiers and one DS2 amplifier. Each amplifier converts the P and N rail RZ data from the Encoder and Error Control logic into a balanced bipolar waveform. Waveshape conditioning and output level is fixed at the DS1 and DS1C rate but the DS2 output can be selected from among HI (high level), DSX (cross-connect), and LO (simulates twice the maximum DSX cable length plus 6 dB of flat loss) level outputs.

DETAILED SYSTEM OPERATION

THE FOLLOWING PARAGRAPHS CONTAIN A STEP-BY-STEP FUNCTIONAL ANALYSIS OF THE TEST SET. REFER TO FIG.6-1 FOR THE OVERALL FUNCTIONAL DESCRIPTION OF THE TEST SET. REFERENCE IS ALSO MADE THROUGHOUT THIS SECTION TO OTHER SPECIFIC SCHEMATIC DIAGRAMS, COMPONENT LOCATIONS, AND INTERCONNECTION DIAGRAMS THAT ARE LISTED IN SECTION 6.

REFERENCES TO INDIVIDUAL CIRCUIT COMPONENTS IN SCHEMATIC DIAGRAMS ARE MADE BY USING AN ALPHANUMERIC DESIGNATION FOLLOWED BY A PIN NUMBER, WHERE APPLICABLE. A TEST REFERENCE TO U24-6, FOR EXAMPLE, INDICATES PIN 6 OF THE LOGIC ELEMENT U24.

PATTERN GENERATOR THEORY OF OPERATION

EACH OF THE THREE CRYSTAL OSCILLATORS ON THIS PC BOARD CONSISTS OF AN EMITTER FOLLOWER WHOSE OUTPUT IS COUPLED TO A COMMON BASE CONFIGURED AMPLIFIER VIA A SERIES NETWORK CONSISTING OF A CRYSTAL AND VARIABLE CAPACITOR. THE COMMON BASE AMPLIFIER IS COUPLED BACK TO THE EMITTER FOLLOWER DRIVER VIA A D.C. COUPLED BUFFER STAGE. THE FREQUENCIES OF THE OSCILLATORS ARE ADJUSTED BY THE VARIABLE CAPACITORS (C3, C12, AND C19). THE OUTPUT WAVEFORMS ARE CONVERTED INTO A 50% DUTY CYCLE CLOCK BY THE LINE RECEIVERS AT U24 AND U25. THE SYMMETRY IS ADJUSTED INDIVIDUALLY BY THE VARIABLE RESISTORS (R15, R11, AND R38).

THE BASIC PSEUDORANDOM SEQUENCE GENERATOR CONSISTS OF A SELF-STARTING 20-STAGE SHIFT REGISTER (U12, U7, U1, U3, AND U9) WHOSE INPUT IS THE EXCLUSIVE-OR OF THE OUTPUT FROM STAGE 17 AND 20.

THE OUTPUT SEQUENCE IS TAKEN FROM STAGE 20 AND IS MODIFIED DURING THE MUX ON MODE BY THE LOGIC AT U2, U4, AND U8. THIS MODIFICATION FORCES THE FINAL DATA OUTPUT TO A LOGICAL "1" WHENEVER THE NEXT 14 BITS OF THE SEQUENCE ARE A LOGICAL "0".

THE DATA FROM U8-1 ARE FED INTO A 4-BIT SHIFT REGISTER AT U20 WITH THE OUTPUT BEING TAKEN FROM U20-2. THESE DATA, AFTER BEING INVERTED BY U34, BECOME THE BASIC FIRST LEVEL DATA SEQUENCE. THE 4-BIT SHIFT REGISTER IS PART OF THE SINGLE BIT ERROR INJECTED LOGIC. A BIT ERROR CAN ONLY BE INJECTED INTO THE DATA AT POINTS WHICH WILL NOT CREATE MORE THAN 14 ZEROS. THIS IS ASSURED BY THE EXCLUSIVE -OR LOGIC AT U28 WHICH IS USED TO DETECT THE PRESENCE OF THREE CONSECUTIVE 1'S OR THREE CONSECUTIVE 0'S IN THE SEQUENCE. IF THREE OF A KIND HAVE BEEN DETECTED AND AN ERROR INJECT HAS BEEN REQUESTED (U27-9 IS A LOGICAL 1), THEN THE MIDDLE BIT OF THE THREE IS INVERTED, THUS CREATING A SINGLE BIT ERROR IN THE SEQUENCE.

THE MFC BIT GENERATOR IS FORMED BY TWO DATA SELECTORS AND TWO SEQUENCE COUNTERS. THE FOUR M-BITS ARE FORMED BY THE DATA SELECTOR AT U38 WHICH IS CONTROLLED BY THE COUNTER AT U30. THE M-BIT SEQUENCE (011X) CHANGES STATE EACH SUB-FRAME DURING THE F1 TIME SLOT. THIS SEQUENCE OF BITS IS FURTHER MULTIPLEXED WITH THE C AND F BITS AT U17. THE 6-STAGE COUNTER AT U15 AND U10 CONTROLS THE U17 DATA SELECTOR FOR PROPER SEQUENCING.

THE C-BITS ARE USED AS MARKERS TO INDICATE THAT A STUFFED BIT HAS BEEN INSERTED INTO THE DEDICATED TIME SLOT WITHIN THE DATA FIELD. ALTHOUGH THE ACTUAL STUFFING IS ACCOMPLISHED ON THE MUX CONTROL PCB, THE CONTROLLING SIGNALS ARE GENERATED ON THE PATTERN GENERATOR PCB. THE SIGNALS CONTROLLING THIS OPERATION ARE THE C-BIT, CN3, F1, AND STUFF CLEAR. THE REQUEST FOR

A STUFF IS GENERATED BY AN ASYNCHRONOUS OSCILLATOR (U6) OPERATING AT EITHER 2264 Hz OR 1796 Hz FOR DS1C OR DS2, RESPECTIVELY. THE RISING EDGE OF THE OSCILLATOR WAVEFORM (TP-5) IS USED TO CLOCK THE Q OUTPUT OF THE FLIP-FLOP AT U5 TO A LOGICAL 1 (STUFF REQUEST).

THE C-BIT (TP-6) IS GENERATED WHEN THE STUFF REQUEST SIGNAL AT U5-9 IS SAMPLED DURING THE (M1 + M3) DECODES OR THE M1 DECODE FOR DS1C AND DS2, RESPECTIVELY.

PATTERN GENERATOR - INPUT/OUTPUT SIGNAL DESIGNATIONS

DS1(1) --- FRONT-PANEL CONTROL SIGNAL THAT IS ENABLED WHEN AT GROUND. SELECTS THE 1.544 MHz CLOCK.

DS1C(1)--- FRONT-PANEL CONTROL SIGNAL THAT IS ENABLED WHEN AT GROUND. SELECTS THE 3.152 MHz CRYSTAL OSCILLATOR, THE 2264 Hz STUFF OSCILLATOR, AND THE DS1C CONTROL BIT SEQUENCE.

DS2(1)--- SAME AS DS1C(1) EXCEPT SELECTS THE 6.132 MHz OSCILLATOR, THE 1796 Hz STUFF OSCILLATOR, AND THE DS2 CONTROL BIT SEQUENCE.

CLOCK--- OUTPUT CLOCK SIGNAL AT THE SELECTED DS RATE.

PR--- PSEUDORANDOM WORD SYNC. THIS SYNC OCCURS ONCE PER SEQUENCE.

PN CLOCK--- INPUT CLOCK FROM THE MUX CONTROL PCB. THIS 1.544 MHz CLOCK IS USED TO CLOCK THE PN GENERATOR.

ONES DATA--- FRONT-PANEL PUSHBUTTON (ONES) INPUT THAT IS ENABLED WHEN AT GROUND. REPLACES THE PN SEQUENCE WITH ALL ONES DATA.

DATA -1 --- OUTPUT DATA PATTERN AT 1.544 M/BITS RATE.

BPV SYNC--- INPUT SYNC PULSE THAT MARKS OCCURENCE OF A BI-POLAR VIOLATION IN THE BIPOLAR OUTPUT.

ERRORS--- REAR-PANEL SYNC OUTPUT THAT MARKS OCCURENCE OF EITHER A SINGLE BIT ERROR OR BIPOLAR VIOLATIONS.

SINGLE BIT ERRORS--- FRONT-PANEL PUSHBUTTON INPUT THAT INITIATES THE INSERTION OF A BIT ERROR INTO THE PSEUDORANDOM SEQUENCE.

X-BIT --- FRONT-PANEL PUSHBUTTON INPUT THAT CONTROLS THE TRANS-MITTED LOGIC LEVEL OF THE M4 CONTROL BIT WITHIN THE DS1C AND DS2 SEQUENCES.

C-BIT --- OUTPUT SIGNAL THAT IS USED BY THE MUX CONTROL PCB TO INITIATE THE STUFFING OF THE DS1 CHANNELS THAT FORM THE DS1C AND DS2 OUTPUTS.

CN3 --- OUTPUT SIGNAL THAT MARKS THE THIRD C-BIT LOCATION WITHIN EACH SUB-FRAME.

F1--- SIGNAL THAT MARKS THE POSITIONS OF THE F1 CONTROL BITS.

MFC --- INVERTED CONTROL BIT DATA COMPRISED OF M, F, AND C BITS. THESE ARE THE OVERHEAD BITS WHICH ARE MULTIPLEXED INTO THE DS1C AND DS2 DATA PATTERNS.

ZERO INH --- INPUT CONTROL SIGNAL THAT INHIBITS THE 15 ZERO SUPPRESSION LOGIC (CONTROLLED BY FRONT-PANEL MUX ON/OFF PUSHBUTTON).

F1, M12 Test Points --- Input when grounded, will cause the F1 or the M1 and M2 control bits to become logic zeros, respectively. These inputs are used only for test purposes.

E5 --- Input signal that occurs during each overhead bit location.

M-Bit--- Rear-panel output, marks location of the M1 overhead bit in DS1C and DS2 sequences.

Multiplexer Control (MUX ON)

The DS2 and DS1C gapped clocks at U6-3 (test point 8) are formed by inhibiting from the incoming clock a single clock pulse each 49th or 53rd time period, respectively. A two-stage counter at U13 and U14 and associated decoding logic at U2 and U10 are used to determine when the 49th and 53rd time slot is present.

The flip-flop at U1 is used to inhibit a clock during that time, thus forming a gapped clock. The frequencies of the DS1C and DS2 gapped clocks are 3.0925 MHz and 6.1832 MHz, respectively. These clocks are divided by either 2 or 4 by the counter located at U21, U20, and U19. After the division, the resulting frequency for the DS1C and DS2, is 1.546246 MHz and 1.54579 MHz, respectively.

Before these clocks can be used to drive the pattern generator logic, they need to be further processed to lower each one to the required 1.544 MHz rate. To lower the frequencies of these clocks, a single pulse is inhibited from the clocks at a rate of 2264 Hz or 1796 Hz. The logic which controls this function

IS LOCATED AT U8, U7, U27, U36, U18, AND U1. THIS LOGIC INITIATES A STUFF REQUEST AT THE APPROPRIATE TIME FOR THE DS1C AND DS2 SIGNALS. ONCE THE STUFF REQUEST HAS BEEN GENERATED AND DETECTED BY U31, THE LOGIC AT U1, U18, AND U20 WILL INHIBIT ONE CLOCK PULSE FROM THE CLOCK OUTPUT OF U19-8. THIS RESULTS IN THE REQUIRED 1.544 MHz CLOCK SIGNAL GOING TO THE PATTERN GENERATOR. THE RETURNING DATA FROM THE PATTERN GENERATOR, DATA 1, WILL NOW BE AT A 1.544 MB/S RATE AND ARE READY FOR PROCESSING BY THE MULTIPLEXER LOGIC. MULTIPLE DATA PATTERNS ARE FORMED BY APPLYING THE INPUT DATA TO A FOUR BIT SHIFT REGISTER LOCATED AT U29. THE DATA TAKEN FROM U29-15 ARE INDICATED AT CHANNEL 1, THE INVERTED DATA TAKEN FROM U29-11 ARE INDICATED AT CHANNEL 2. THE THIRD CHANNEL INDICATES THE DATA AT U29-7 AND THE FOURTH CHANNEL INDICATES THE INVERTED DATA AT U29-3.

A DS2 SIGNAL IS FORMED BY MULTIPLEXING THE FOUR DS1 RATE PATTERNS TOGETHER. DATA FROM CHANNEL 1 (U29-15) ARE SAMPLED FIRST; CHANNEL 2 (U29-11) IS SAMPLED SECOND; CHANNEL 3 (U29-7) IS SAMPLED THIRD, AND CHANNEL 4 (U29-3) IS SAMPLED FOURTH. THE FORMED SEQUENCE IS D1, D2, D3, D4. . . . D1, D2, D3, D4. THIS INTERLEAVING CONTINUES FOR 48 TIME SLOTS. DURING THE 49TH TIME SLOT, THE CONTROL BIT FROM THE PATTERN GENERATOR WILL BE INSERTED. FOLLOWING THE CONTROL BIT, THE MULTIPLEXING SEQUENCE BEGINS AS BEFORE WITH CHANNEL 1. THE SAMPLING SIGNALS DERIVED AT GATES U24 AND U15 CAN BE OBSERVED AT TEST POINTS 1 THROUGH 5.

THE DS1C SIGNAL IS FORMED IN A LIKE MANNER, EXCEPT THAT ONLY CHANNEL 1 AND CHANNEL 2 ARE MULTIPLEXED TOGETHER, FORMING THE SEQUENCE D1, D2, D1, D2 . . . ANOTHER DIFFERENCE THAT OCCURS WITH DS1C MULTIPLEXING IS THAT ONCE THE MULTIPLIED BIT STREAM IS FORMED, IT IS SCRAMBLED IN THE SINGLE

STAGE SCRAMBLER LOCATED AT U17 AND U26. THE OUTPUT OF THE SCRAMBLER (U17-8) IS EQUAL TO THE MODULO-2 SUM OF THE PRESENT INPUT BIT AND THE PRECEEDING OUTPUT BIT. THE CONTROL BITS ARE MULTIPLEXED WITH THE SCRAMBLED DATA AT U25 WHERE THE RESULTING BIT STREAM IS RELATCHED BY U26.

THE INSERTION OF THE STUFFING BITS INTO THE INFORMATION DATA FIELD FOLLOWS A BELL SYSTEM DEFINED SET OF RULES. THE DS1C STUFFING OCCURS IN THE FOLLOWING MANNER: CHANNEL 1 STUFFING MAY OCCUR ONLY IN THE FIRST OR THIRD SUB-FRAMES, IN THE THIRD CHANNEL 1 TIME SLOT LOCATION FOLLOWING THE C13 BIT. CHANNEL 2 MAY BE STUFFED ONLY IN SUBFRAME 2 AND 4, IN THE THIRD CHANNEL 2 TIME SLOT LOCATION FOLLOWING THE C23 DATA BIT. THE DS2 CRITERIA ARE SLIGHTLY DIFFERENT IN THAT CHANNEL 1 CAN ONLY BE STUFFED IN SUBFRAME ONE, DURING THE FIRST TIME SLOT FOLLOWING THE F1 BIT. CHANNEL 2 CAN ONLY BE STUFFED DURING THE SECOND TIME SLOT FOLLOWING THE F1 BIT AND CHANNEL 3 CAN ONLY BE STUFFED IN THE THIRD SUBFRAME, DURING THE THIRD TIME SLOT FOLLOWING THE F1 BIT AND LIKEWISE THE FOURTH CHANNEL CAN ONLY BE STUFFED IN THE FOURTH SUBFRAME DURING THE FOURTH TIME SLOT FOLLOWING THE F1 BIT. THESE INSERTION TIMES ARE CONTROLLED BY THE LOGIC AT U18, U8, U27, AND U7 AND ARE DERIVED FROM THE F1 BIT, THE C BIT DECODE, AND THE CN3 BIT WHICH ARE RECEIVED FROM THE PATTERN GENERATOR BOARD. THE COUNTER AT U8 IS USED DURING THE DS1C MODE TO DETERMINE WHEN THREE TIME SLOTS HAVE OCCURRED AFTER THE CN3 BIT IN ORDER THAT THE PROPER LOCATION IS KNOWN FOR STUFFING. THE DS2 STUFFING IS PERFORMED ONLY BY OBSERVING WHEN THE F1 BIT HAS OCCURRED AND THAT THE C BIT DECODE HAS OCCURRED.

ONCE A STUFF REQUEST HAS BEEN GENERATED THE FLIP-FLOPS AT U31 WILL GATE INTO THE MULTIPLEXER EITHER THE DATA FROM U29 OR THE DELAYED DATA FROM U30. THE CHOICE OF DATA IS SUCH THAT THE STUFF LOCATION CONTAINS THE SAME BIT OF DATA THAT WAS LAST TRANSMITTED FOR THE CHANNEL THAT IS CURRENTLY BEING STUFFED. THE STUFFING OPERATION IS SUCH THAT A STUFF REQUEST WILL BE GENERATED FOR ALL CHANNELS IN A GIVEN FRAME; THAT IS, IF DS1C CHANNEL 1 IS BEING STUFFED, THEN CHANNEL 2 WILL BE STUFFED IN THE FOLLOWING SUBFRAME. IN THE CASE OF DS1C, IT WOULD BE POSSIBLE BUT NOT NECESSARY TO STUFF CHANNEL 1 INTO SUBFRAME 1, CHANNEL 2 INTO SUBFRAME 2 AND AGAIN STUFF CHANNEL 1 INTO SUBFRAME 3, FOLLOWED BY THE STUFFING OF CHANNEL 2 INTO SUBFRAME 4. AFTER ALL REQUIRED CHANNELS HAVE BEEN STUFFED, THE REGISTER AT U31 WILL BE CLEARED BY THE SIGNAL STUFF CLEAR WHICH IS RECEIVED FROM THE PATTERN GENERATOR. THIS SIGNAL IS, IN THE CASE OF DS1C, EITHER THE M1 OR THE M3 DECODE AND, IN THE CASE OF DS2, THE M2 DECODE. THESE DECODES, M1 AND M3 ARE THE FIRST BIT OF SUBFRAME 1 OR SUBFRAME 3, RESPECTIVELY.

MULTIPLEXER CONTROL (MUX ON) - INPUT/OUTPUT DESIGNATIONS

CLOCK --- THIS IS THE MAIN SIGNAL CLOCK GENERATED BY THE CRYSTAL OSCILLATORS LOCATED ON THE PATTERN GENERATOR BOARD.

DS1C --- THIS SIGNAL IS ACTIVATED TO A LOGIC "0" BY THE FRONT-PANEL PUSHBUTTON.

DS1 --- THIS SIGNAL IS THE SAME AS DS1C.

DS2 --- THIS SINGAL IS THE SAME AS DS1C.

DATA 1--- THE PSEUDORANDOM SEQUENCE FROM THE PATTERN GENERATOR BOARD.

PN CLOCK --- THE CLOCK WHICH IS GENERATED ON THE PC BOARD AND IS SENT TO THE PATTERN GENERATOR BOARD. THE AVERAGE FREQUENCY OF THIS CLOCK IS 1.544 MHz.

DS CLOCK --- THE SAME CLOCK AS RECEIVED FROM THE CRYSTAL OSCILLATORS AND IS SENT TO THE ENCODER AND ERROR CONTROL PC BOARD.

DS DATA --- THE FINAL OUTPUT DATA FROM THIS PC BOARD AND IS SENT TO THE ENCODER AND ERROR CONTROL PC BOARD.

OH BITS --- THE CONTROL BITS (M,F,C) AND ARE DERIVED ON THE PATTERN GENERATOR BOARD AND SENT TO THIS BOARD FOR MULTIPLEXING INTO THE DS DATA STREAM.

F1 BIT --- A CONTROL BIT FROM THE PATTERN GENERATOR AND IS USED ONLY IN THE DS2 AND DS1C MODE.

C BIT DECODE --- A CONTROL BIT INPUT WHICH IS USED ONLY IN THE DS1C AND DS2 MODE.

CN3 BIT --- A CONTROL BIT WHICH IS ONLY IN THE DS1C AND DS2 MODES.

STUFF CLEAR --- A CONTROL SIGNAL WHICH IS USED ONLY IN THE DS1C AND DS2 MODES. DURING DS1C THIS SIGNAL IS EITHER THE M1 OR THE M3 DECODE. DURING DS2 THIS SIGNAL IS ONLY THE M1 DECODE.

E5 --- A CONTROL SIGNAL OUTPUT GOING TO THE PATTERN GENERATOR PC BOARD. THE PATTERN GENERATOR USES THIS SIGNAL TO INITIATE AN OVERHEAD BIT UPDATE.

TP-1--- E5, OH BIT SAMPLE TIME.

TP-2--- E1, CHANNEL 1 SAMPLE ENABLE.

TP-3--- E2, CHANNEL 2 SAMPLE ENABLE.

TP-4--- E3, CHANNEL 3 SAMPLE ENABLE.

TP-5--- E4, CHANNEL 4 SAMPLE ENABLE.

TP-6--- PN CLOCK, CAPPED FOR AVERAGE 1.544 MHZ RATE.

TP-7--- PN CLOCK PRIOR TO GAPPING.

MUTIPLEXER CONTROL (MUX OFF)

CLOCK AND DATA RECEIVED FROM THE PATTERN GENERATOR ARE PASSED THROUGH THIS PCB UNALTERED. ALL MULTIPLEXING AND SCRAMBLING FUNCTIONS ARE INHIBITED.

ENCODER AND ERROR CONTROL

THE LOGIC OF THE ENCODING SECTION CONSTISTS OF A SIX-STAGE REGISTER (U4 AND U10) AND A ZERO DETECTOR LOCATED AT U9. THE SIX-ZERO DETECTOR IS ONLY ENABLED DURING THE DS2 MODE. THE FLIP-FLOP AT U22 CHANGES STATES EACH TIME A LOGICAL 1 OCCURS IN THE DATA SEQUENCE. THE OUTPUT OF THE FLIP-FLOP CONTROLS THE GATES (U28), WHOSE OUTPUTS ARE THE P AND N RAIL RZ PULSES, IN SUCH A WAY THAT FOR A SERIES OF LOGICAL ONES AT THE INPUT, THE P AND N RAILS WILL ALTERNATELY OUTPUT THE PULSE. THIS IS IN CONFORMANCE WITH THE AMI RULES.

WHEN A BIPOLAR ERROR IS REQUESTED, THE SIGNAL AT THE EXCLUSIVE -OR GATE (U29-2) IS INVERTED CAUSING THE INPUT TO THE JK FLIP-FLOP TO BE INCORRECT. THIS WILL CAUSE THE BIPOLAR OUTPUT TO CONTAIN A PULSE OF THE SAME POLARITY AS THE PREVIOUS OUTPUT PULSE, THUS CREATING A BIPOLAR VIOLATION. DURING THE DS2 MODE, WHEN THE B6ZS CODE IS ENABLED, THE SIX-ZERO DETECTOR LOCATED AT U9 MONITORS THE STATUS OF THE SIX-STAGE REGISTER. WHEN SIX ZEROS ARE DETECTED IN THE REGISTER, U9-8 WILL GO LOW, INPUTING INTO THE REGISTER THE CONDITION 011011. THIS SIX ZERO DETECTED SIGNAL IS ALSO FED INTO A FOUR-BIT CONTROL REGISTER AT U10 AND U16. THE OUTPUT OF THIS CONTROL BIT REGISTER IS THE PATTERN 001001. WHEN THIS PATTERN AND THE SUBSTITUTED PATTERN 011011 ARE OR'ED TOGETHER AT U27 AND FED INTO THE JK FLIP-FLOP AT U22, THE B6ZS CODE (OVBOVB) IS FORMED. THE LOGIC AT U23, U16, U22, AND U17 FORM AN INHIBIT SINGAL THAT BLOCKS AN ERROR REQUEST FROM BEING ACKNOWLEDGED WHILE THE B6ZS CODE IS BEING TRANSMITTED. IF THIS IS NOT DONE, THE REQUESTED ERROR WOULD BE ALLOWED TO OCCUR DURING THE B6ZS CODE CAUSING BOTH BIT ERRORS AND VIOLATIONS TO OCCUR. THE TEST SET IS DESIGNED IN SUCH A WAY THAT NO ERRORS WILL OCCUR DURING THE B6ZS SUBSTITUTION. THE ERROR INSERTION LOGIC CONSISTS OF A COUNTER-CHAIN OF 8 DECADE STAGES, A TWO-STAGE COUNTDOWN COUNTER AND A PROM WHICH CONTAIN THE PRESET DATA FOR THE COUNTDOWN COUNTER. THE CIRCUIT PROVIDES EVENLY SPACED ERRORS WITHIN THE SELECTED DECADE RANGE. FOR AN EXAMPLE OF HOW THIS IS DONE, CONSIDER THE CASE WHEN AN ERROR RATE OF 4×10^{-3} IS DESIRED. THE PROM ADDRESS IS SELECTED BY THE LEFT-HAND THUMBWHEEL SWITCH (K) ON THE FRONT PANEL, WHICH WOULD BE A 4. THE FOURTH ADDRESS WITHIN THE PROM AS SHOWN IN TABLE 4-2 IS A DECIMAL NUMBER 23. THIS NUMBER IS LOADED INTO THE COUNTDOWN COUNTERS AT U12 AND U6. THE 10^{-3} RANGE IS SELECTED BY MULTIPLEX SWITCHES (U13 AND U19) WHICH ARE CONTROLLED BY THE RIGHT-HAND THUMBWHEEL SWITCH (N). THE MULTIPLEX SWITCH (U13), FOR AN INPUT OF N = 3, WILL SELECT THE 10^{-3} FROM U14.

TABLE 4-2
CONTENTS OF PROM

K	ADDRESS (BCD)	DATA (DECIMAL)	DATA B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
1	0001	90	1	0	0	1	0	0	0	0
2	0010	47	0	1	0	0	1	1	1	1
3	0011	31	0	0	1	1	0	0	0	1
4	0100	23	0	0	1	0	0	0	1	1
5	0101	19	0	0	0	1	1	0	0	1
6	0110	16	0	0	0	1	0	1	1	0
7	0111	14	0	0	0	1	0	1	0	0
8	1000	12	0	0	0	1	0	0	1	0
9	1001	11	0	0	0	1	0	0	0	1

THE U19 MULTIPLEX WILL RECIEVE THE DIVIDE-BY-TEN SIGNAL FROM U26. IT SHOULD BE NOTED THAT THE OUTPUT OF U19 IS USED AS THE CLOCK SIGNAL FOR U12 AND U6 DECADE COUNTDOWN COUNTERS. WHEREAS, THE OUTPUT OF U13 IS PASSED THROUGH A ONESHOT EDGE DETECT CIRCUIT WHOSE OUTPUT IS USED TO LOAD THE CONTENTS OF THE PROM INTO THE DECADE COUNTDOWN COUNTERS. AT THE END OF EACH 1,000 CLOCKS, (10^3), THE COUNTDOWN COUNTERS ARE RELOADED WITH THE CONTENTS OF THE PROM (23 IN THIS CASE). ALSO, THE COUNTERS UPON REACHING THEIR MINIMUM COUNT WILL RELOAD THEMSELVES VIA THE SIGNAL GENERATED IN THE U1 EDGE DETECT CIRCUIT. THUS, IN A WINDOW OF 1,000 BITS, THE COUNTDOWN COUNTERS WILL BE ABLE TO RELOAD AND COUNT DOWN FOUR TIMES. AFTER COUNTING DOWN 4 TIMES THE COUNTDOWN COUNTERS WILL AGAIN BE LOADED. BUT BEFORE THEY CAN REACH THEIR MINIMUM COUNT, THEY ARE AGAIN

LOADED BY THE 1,000 BIT DETECTED SIGNAL. THEREFORE, THIS METHOD PROVIDES VERY ACCURATE ERROR INSERTIONS IN A GIVEN WINDOW. IN THIS CASE, 4 ERRORS IN A 1,000 BIT WINDOW SPACED 230 BITS APART. IN ADDITION TO THE ACCURACY OF THE ERROR INSERTION, THE DISTRIBUTION IS ALSO GUARANTEED AS REQUIRED BY THE SPECIFICATION.

ENCODER AND ERROR CONTROL - INPUT/OUTPUT DESIGNATIONS

THE DS DATA --- DATA FROM THE MUX CONTROL. ITS CHARACTERISTICS ARE DESCRIBED UNDER THE MUX CONTROL PC BOARD.

DS CLOCK --- CLOCK FROM THE MUX CONTROL BOARD.

P RAIL --- RZ PULSE WHICH IS SENT TO THE OUTPUT AMPLIFIER TO DRIVE THE OUTPUT IN THE POSITIVE DIRECTION.

N RAIL --- SIGNAL WHICH IS SENT TO THE OUTPUT AMPLIFIER CAUSING THE OUTPUT TO DRIVE NEGATIVE.

BPV SYNC --- A SYNC PULSE THAT IS SENT TO THE PATTERN GENERATORS. ONE PULSE IS GENERATED EACH TIME AN ERROR IS INSERTED INTO THE DATA STREAM. K1, K2, K4, AND K8 ARE THE VALUES IN BCD CODING FOR THE VALUE K, AS SHOWN ON THE FRONT PANEL. THE DECIMAL VALUE OF K CAN RANGE FROM 1 TO 9. N1, N2, AND N4 ARE THE BCD VALUES FOR THE VALUE N, AS SHOWN ON THE FRONT PANEL. N CAN HAVE A DECIMAL VALUE OF 3 THROUGH 8.

ONES --- THE ONES INPUT WHEN SELECTED TO A LOGIC "0" WILL CAUSE THE ALL ONES DATA TO BE INSERTED INTO THE OUTPUT. THIS SIGNAL IS

USED WHEN ADJUSTING THE POWER IN THE DS2 OUTPUT WAVEFORM. IT OVERRIDES ALL CONTROL BITS AND IS, THEREFORE, NOT USEFUL IN THE NORMAL MODES. THE SWITCH FOR THIS SIGNAL IS LOCATED ON THE REAR PANEL.

DS2--- THIS SIGNAL, WHEN LOW, ACTIVATES THE SIX ZERO DETECTOR USED FOR B6ZS ENCODING.

INJ--- THE INJ SIGNAL IS USED TO ENABLE THE COUNTDOWN COUNTER-CHAIN FOR ERROR INSERTION.

TP-1--- 6 ZERO DETECT SIGNAL, ACTIVE DS2 ONLY.

TP-2--- SELECTED DECADE COUNT USED TO ESTABLISH THE NUMBER OF BITS OVER WHICH BIPOLAR ERRORS WILL BE DISTRIBUTED.

TP-3--- SELECTED DECADE COUNT USED TO DRIVE COUNTDOWN COUNTERS. THE DECADE SELECTED MULTIPLIED BY THE CONTENTS OF THE PROM YIELDS THE ERROR SPACING.

OUTPUT AMPLIFIER - THEORY OF OPERATION

DS1/DS1C AMPLIFIER --- THE P AND N SIGNALS ARE SLICED FOR WAVESHAPE SYMMETRY BY THE LINE RECEIVER (U1). THE SLICING LEVEL IS CONTROLLED BY ADJUSTING VARIABLE RESISTORS (R42/R45). EACH AMPLIFIER IS PARALLEL DRIVEN BY THE LINE RECEIVER OUTPUT AND CONSISTS OF TWO TRANSISTORS WHICH ARE ALTERNATELY SWITCHED ON AND OFF BY THE P AND N RAILS. THE BIPOLAR WAVEFORM IS FORMED BY THE SWITCHING CURRENTS ALTERNATELY FLOWING IN THE OUTPUT TRANSFORMER. A BALANCED BRIDGED-T NETWORK SHAPES THE NORMALLY RECTANGULAR WAVESHAPE INTO ONE WITH THE DESIRABLE FALLING EDGE UNDERSHOOT WHILE MAINTAINING A HIGH RETURN LOSS.

DURING A REDUCE LEVEL TEST, THE VOLTAGE SUPPLYING EACH AMPLIFIER IS REDUCED VIA Q6 TO A VALUE THAT RESULTS IN AN OUTPUT POWER DROP OF 24 DB. THE LOW LEVEL SUPPLY VOLTAGE IS CONTROLLED BY R56.

DS2 AMPLIFIER --- THE DS2 AMPLIFIER IS THE SAME BASIC LINE RECEIVER/DRIVER CONFIGURATION AS IS USED IN THE DS1/DS1C AMPLIFIER. FOLLOWING THE Q1, Q2, T1 DRIVER CIRCUITS ARE SELECTABLE BRIDGED-T NETWORKS WHICH SHAPE THE HIGH LEVEL SIGNAL INTO THE DSX AND LO WAVEFORMS. THE NETWORKS ARE BUFFERED BY AN EMITTER FOLLOWER STAGE Q15 WHICH HAS AN OUTPUT IMPEDANCE OF 110 OHMS. TRANSFORMER T2 CONVERTS THE SINGLE-ENDED EMITTER FOLLOWER OUTPUT INTO A BALANCED 110 OHM SOURCE.

LOST POWER MONITOR --- A CURRENT LIMITED AC VOLTAGE TAKEN FROM THE SECONDARY OF THE POWER TRANSISTOR IS APPLIED TO THIS BOARD VIA AN OPTOCOUPLER (U8). THE 60 HZ TRANSITIONS KEEP THE ONE SHORT (U3) IN A TRIGGER STATE. WHEN THE AC POWER IS LOST AND THEN RESTORED, U8-13 MAKES A LOW TO HIGH TRANSITION, SETTING THE FLIP-FLOP U7-11.

OUTPUT AMPLIFIER - INPUT/OUTPUT DESIGNATIONS

DS2(L) --- CONTROL SIGNAL THAT IS ACTIVE LOW. ROUTES THE HIGH LEVEL DS2 SIGNAL TO FINAL OUTPUT DRIVER.

DS2-DSX --- CONTROL SIGNAL THAT IS ACTIVE LOW. ROUTES THE HIGH LEVEL DS2 SIGNAL THROUGH A SIMPLE LBO NETWORK PRIOR TO FINAL DRIVER.

DS2-LO--- CONTROL SIGNAL THAT IS ACTIVE LOW. ROUTES THE DSX SIGNAL THROUGH AN ADDITIONAL LBO NETWORK PRIOR TO FINAL DRIVER.

REDUCE LEVEL --- CONTROL SIGNAL THAT IS ACTIVE HIGH. REDUCES SUPPLY VOLTAGE TO DS1(CHANNEL 1) AMPLIFIER.

A.C. --- CURRENT LIMITED A.C. INPUT FROM POWER SUPPLY TRANSFORMER.

LOST POWER --- LED DRIVE SIGNAL TO FRONT-PANEL LOST POWER INDICATOR THAT IS ACTIVE HIGH.

RESET --- CONTROL SIGNAL THAT IS ACTIVE LOW FROM FRONT PANEL. USED TO RESET LOST POWER INDICATOR.

P-RAIL, N-RAIL --- RZ DATA INPUTS THAT ARE USED TO FORM THE BIPOLAR WAVEFORM.

DS1/DS1C --- BALANCED BIPOLAR OUTPUT SIGNALS.

DS2 OUTPUT--- BALANCED B6ZS OUTPUT SIGNAL.

SECTION 5
MAINTENANCE

GENERAL

This section contains the preventative and corrective maintenance procedures for the S5102 Error Rate Test Set (Transmitter).

Maintenance support data in the form of diagrams, tables, and descriptive material are provided in the other sections of this manual. A discussion of circuit theory is presented in Section 4. The latter part of this section contains individual parts lists for each of the four circuit boards and the chassis (Tables 5-3 through 5-9). Schematic diagrams, component locations, and internal wiring diagrams are located in Section 6. Refer to Appendix A for DC power supply information.

Theuser should be thoroughly familiar with the Test Set capabilities, theory of operation, and operating procedures before attempting any maintenance or troubleshooting procedures. Table 5-1 lists the required maintenance test equipment.

Component Location

The physical location of the major components in the Test Set chassis are shown in Figure 1-1. Figures 6-2 through 6-5 show

TABLE 5-1
TEST EQUIPMENT REQUIRED FOR MAINTENANCE (BUT NOT SUPPLIED)

ITEM	TYPE	PURPOSE
OSCILLOSCOPE	TEKTRONIX MODEL 475 OR EQUIVALENT	MONITORING WAVEFOREMS, SIGNAL LEVEL, ETC.
DIGITAL VOLTMETER	SIMPSON MODEL 461 OR EQUIVALENT DIGITAL MULTIMETER	PRECISION VOLTAGE READINGS DURING ALIGNMENT PROCEDURES
ELECTRONIC COUNTER	HP-5383A OR EQUIVALENT	FREQUENCY OF PERIOD MEASUREMENTS
EXTENDER CARD	TAU-TRON P/N 1-7219	PC CARD ACCESS 22 PIN
EXTENDER CARD	TAU-TRON P/N 1-7195	D.C CARD ACCESS DUAL 28 PIN

THE VARIOUS COMPONENTS ON CIRCUIT BOARDS A1, A2, A3, AND A4, RESPECTIVELY.

Preventive Maintenance

Preventative maintenance includes the performance of checks and services, which prevent or minimize down time of the equipment. Through utilization of solid-state circuitry, the checks and services are simplified, and may be limited to visual inspection for defective components, loose hardware and/or accumulation of dust within the unit at critical areas.

Minor Repair Procedures

Minor repair procedures for the Test Set are limited to items such as indicator and fuse replacement. The panel fuse (3/4 ampere, slo-blo, 3AG) is replaced at the unit front panel by removing the power cable, sliding the plastic door to the left, pulling the tab guard and ejecting the fuse. Push the replacement fuse into the holder, slide the door to the right and replace the power cable. Note: If a new fuse blows immediately after replacement, determine the cause of the problem before inserting another fuse.

Corrective Maintenance

Corrective maintenance of the Test Set consists of repairs or adjustments, that must be made after a malfunction or failure occurs, to restore the unit to normal operation.

CORRECTIVE MAINTENANCE REPAIRS SHOULD ONLY BE ATTEMPED BY QUALIFIED PERSONNEL, KNOWLEDGEABLE IN SOLID-STATE LOGIC AND CIRCUIT THEORY AND, IN PARTICULAR, THOROUGHLY FAMILIAR WITH THE TEST SET THEORY OF OPERATION. NECESSITY FOR CORRECTIVE MAINTENANCE IS INDICATED, WHEN ANY VARIATION FROM THE SPECIFIED OPERATIONAL CRITERIA OF THE UNIT IS NOTED.

ADJUSTMENT PROCEDURES

THE ONLY TEST SET ADJUSTMENTS THAT MAY BE REQUIRED ARE THE DC POWER SUPPLY OUTPUT VOLTAGES, THE TRANSMITTED DATA OUTPUT AMPLITUDE AND SYMMETRY, AND THE FREQUENCY AND WAVEFORM ADJUSTMENTS FOR THE THREE INTERNAL OSCILLATORS.

A: POWER SUPPLY ADJUSTMENTS: REFER TO APPENDIX A FOR +5V AND +12V POWER SUPPLY ADJUSTMENT POINTS ON THE PS1 POWER SUPPLY.

B: TRANSMITTED DATA OUTPUT ADJUSTMENT: THE AMPLITUDE AND SYMMETRY OF THE TRANSMITTED DATA OUTPUT FOR DS1, DS1C, AND DS2 RATES CAN BE ADJUSTED USING THE FOLLOWING PROCEDURE:

1. REMOVE THE TEST SET FROM ITS ENCLOSURE AND MOUNT THE OUTPUT AMPLIFIER BOARD (REFER TO FIG. 1-2) ON A STANDARD DUAL 22-PIN EXTENDER CARD.

2. TURN THE POWER ON AND ALLOW AT LEAST 15 MINUTES BEFORE MAKING ANY ADJUSTMENTS TO THE TEST SET.

3. After the 15 minute stabilization period, the following adjustments may be made with an oscilloscope connected to the respective data output jack. (Refer to Table 5-2).

TABLE 5-2
DATA OUTPUT ADJUSTMENTS

Data Rate	Front-Panel Connector	Amplitude	Symmetry Adjustment	Amplitude Adjustment
DS1/DS1C	J1	± 3V ± 10%	R42/R45	R48/R52
DS1/DS1C	J2	± 3V ± 10%	R42/R45	R57/R61
DS1/DS1C	J3	± 3V ± 10%	R42/R45	R67/R72
DS1/DS1C	J4	± 3V ± 10%	R42/R45	R78/R82
DS2	J5	± 2.1V ±1 DB	R28/31	R22/R23

C: Oscillator Frequency and Waveform Adjustment: The frequency and waveform of each internal oscillator should be checked as required. Each oscillator has been factory-adjusted and frequent re-adjustment should not be required. However, if for any reason an oscillator frequency is not within the allowable tolerance, make the adjustment as follows:

1. Remove the Test Set from its enclosure and mount the Pattern Generator board on a standard dual 22-pin extender card.

2. Turn the power on and allow at least 15 minutes before making any adjustments to the test set.

3. After the 15 minute stabilization period, select the front-panel switch for the output rate to be adjusted. Connect a frequency counter to the CLOCK terminal at the rear of the Test Set and adjust the variable capacitor (C3 -1.544 MHz, C12 -3.152 MHz, or C19 -6.312 MHz) in series with the crystal until the frequency is within tolerance ($\pm$ 50 Hz).

4. Repeat the above steps for any of the remaining oscillators, if their frequencies are out of tolerance.

5. The symmetry of the waveform for each frequency should have a 50% $\pm$ 5% duty cycle as measured at the CLOCK monitor. Adjustments can be made by attaching an oscilloscope to the CLOCK monitor and adjusting resistors R11 (1.544 MHz), R15 (3.152 MHz), and R38 (6.132 MHz) on the Pattern Generator board for 5V $\pm$ .5V (into an open circuit).

Troubleshooting Procedures

Troubleshooting procedures should be performed in a logical sequence to isolate a malfunction to a specific location. Familiarization with the unit will enable the technical personnel to rapidly isolate the problem area. This may be attained with the aid of functional characteristics, circuit theory discussions, and schematic and component

DIAGRAMS PRESENTED IN SECTION 6 OF THIS MANUAL.

MALFUNCTIONS CAN GENERALLY BE LIMITED TO PRINTED CIRCUIT BOARDS PC2 THROUGH PC5 (REFER TO FIG. 1-1). ONCE ISOLATED TO A BOARD, COMPONENTS CAN BE MONITORED FOR CORRECT WAVEFORMS BY USING AN EXTENDER BOARD.

CAUTION: USE CAUTION WHEN MEASURING THE RESISTANCE OF SOLID-STATE DEVICES. THE DEVICES MAY BE DAMAGED BY THE APPLICATION OF VOLTAGES WITH IMPROPER POLARITIES OR BY HIGH SHORT-CIRCUIT CURRENT OF MOST VOLT-OHMMETERS.

IF NORMAL OPERATION OF THE UNIT INDICATES A MALFUNCTION, THE FOLLOWING GENERAL ITEMS SHOULD BE CHECKED BEFORE BEGINNING A TROUBLESHOOTING PROCEDURE:

A. POWER IS APPLIED TO THE UNIT (RED POWER INDICATOR ILLUMINATES).

B. ALL INTERNAL AND EXTERNAL CONNECTORS ARE SECURELY MATED WITH THE PROPER RECEPTACLES.

C. ALL REQUIRED OUTPUT SIGNALS ARE BEING TRANSMITTED FROM THE TEST SET.

D. ALL FRONT-PANEL SWITCHES ARE PROPERLY SET FOR THE PARTICULAR FUNCTION TO BE PERFORMED.

TABLE 5-3

PARTS LIST FOR PATTERN GENERATOR PRINTED CIRCUIT BOARD (P2)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-2120	RES COMP 12 OHM 5P 1/4
0022-2220	RES COMP 22 OHM 5P 1/4
0022-2620	RES COMP 62 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-3100	RES COMP 100 OHM 5P 1/4
0022-3240	RES COMP 240 OHM 5P 1/4
0022-3430	RES COMP 430 OHM 5P 1/4
0022-3470	RES COMP 470 OHM 5P 1/4
0022-3510	RES COMP 510 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4150	RES COMP 1.5 KOHM 5P 1/4
0022-4160	RES COMP 1.6 KOHM 5P 1/4
0022-4180	RES COMP 1.8 KOHM 5P 1/4
0022-4240	RES COMP 2.4 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-4910	RES COMP 9.1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0110-5280	RES MFLM 28 KOHM 1P 1/8W
0110-5340	RES MFLM 34 KOHM 1P 1/8W
0333-3500J	RES VAR 500 OHM 10P 1/2W
0333-4500	RES VAR 5 KOHM 10P 1/2W
1012-0220	CAP CER 20 PF 5P N150C 1
1013-7268	CAP CER 68 PF 10P 100V
1013-8222	CAP CER 22 PF 10P 200V
1013-8368	CAP CER 680 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1014-4610	CAP CER 0.1 MFD 20P 200V
1040-7468	CAP MICA 6800 PF 1P 100V
1059-5253	CAP VAR 9-35 PF PC MNT
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
2112-4148	DIODE GEN PURPOSE IN4148
3224-2369	TRNSTR NPN SWITCHING MPS
3224-4403	TRNSTR NPN AMPLIFIER 2N4
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-4001	IC CMOS MC14001BCP PLSTC
4012-4011	IC CMOS MC14011BCP PLSTC
4012-4012	IC CMOS MC14012BCP PLSTC
4012-4013	IC CMOS MC14013BCP PLSTC
4012-4023	IC CMOS MC14023BCP PLSTC
4012-4027	IC CMOS MC14027BCP PLSTC
4012-4047	IC CMOS MC14047BCP PLSTC
4012-4049	IC CMOS MC14049BCP PLSTC
4012-4512	IC CMOS MC14512BCP PLSTC
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
4012-74LS05	IC TTL SN74LS05N PLSTC
4012-74LS10	IC TTL SN74LS10N PLSTC
4012-74LS123	IC TTL SN74LS123N PLSTC
4012-74LS175	IC TTL SN74LS175N PLSTC
4012-74LS30	IC TTL SN74LS30N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-7416	IC TTL SN7416N PLSTC
4012-75182	IC LINEAR SN75182AN PLST
5023-2339	INDCTR MLD 390 UH 10P
6000-6110	XTAL 5.312 MHZ
6000-6111	XTAL 1.544 MHZ
6000-6127	XTAL 3.152 MHZ
7000-0172	RELAY 5 PIN DIP W172DIP-
8000-9003	PIN PCB CONCORD 10-916-2
9601-0533	S5102TX PATTERN GEN PCB

TABLE 5-4

PARTS LIST FOR MULTIPLEXER CONTROL PRINTED CIRCUIT BOARD (P3)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0822-5100	RES SIP 8PIN 10 KOHM 2P
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS01	IC TTL SN74LS01N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-74LS08	IC TTL SN74LS08N PLSTC
4012-74LS10	IC TTL SN74LS10N PLSTC
4012-74LS11	IC TTL SN74LS11N PLSTC
4012-74LS112	IC TTL SN74LS112N PLSTC
4012-74LS162	IC TTL SN74LS162N PLSTC
4012-74LS175	IC TTL SN74LS175N PLSTC
4012-74LS20	IC TTL SN74LS20N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-74S10	IC TTL SN74S10N PLSTC
4012-74S30	IC TTL SN74S30N PLSTC
4012-7404	IC TTL SN7404N PLSTC
8000-8003	FLAT CABLE 26 POS 28AWG
9601-0532	S5102TX MUX CONTROL PCB

TABLE 5-5

PARTS LIST FOR ENCODER AND ERROR CONTROL PRINTED CIRCUIT BOARD (P4)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0012-3100	RES COMP 100 OHM 5P 1/8
0022-2120	RES COMP 12 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4180	RES COMP 1.3 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0822-5100	RES SIP 8PIN 10 KOHM 2P
1013-8333	CAP CER 330 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS112	IC TTL SN74LS112N PLSTC
4012-74LS175	IC TTL SN74LS175N PLSTC
4012-74LS190	IC TTL SN74LS190N PLSTC
4012-74LS20	IC TTL SN74LS20N PLSTC
4012-74LS27	IC TTL SN74LS27N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-7402	IC TTL SN7402N PLSTC
4012-7404	IC TTL SN7404N PLSTC
4012-74151	IC TTL SN74151N PLSTC
4012-7416	IC TTL SN7416N PLSTC
4012-7430	IC TTL SN7430N PLSTC
4012-7490	IC TTL SN7490N PLSTC
4416-8004	IC PROM P004
4416-3009	IC PROM SIGNETICS 825123
8000-9003	PIN PCB CONCORD 10-516-2
9300-0030	SOCKET IC 16 PIN LOW PRO
9601-0529C	S5102TX ENC/ERR CONTROL

TABLE 5-6

PARTS LIST FOR OUTPUT AMPLIFIER PRINTED CIRCUIT BOARD (P5)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-1560	RES COMP 5.6 OHM 5P 1/4
0022-3100	RES COMP 100 OHM 5P 1/4
0022-3110	RES COMP 110 OHM 5P 1/4
0022-3200	RES COMP 200 OHM 5P 1/4
0022-3270	RES COMP 270 OHM 5P 1/4
0022-3390	RES COMP 390 OHM 5P 1/4
0022-3680	RES COMP 680 OHM 5P 1/4
0022-3750	RES COMP 750 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4130	RES COMP 1.3 KOHM 5P 1/4
0022-4200	RES COMP 2 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-4910	RES COMP 9.1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0022-6150	RES COMP 150 KOHM 5P 1/4
0032-3150	RES COMP 150 OHM 5P 1/2
0042-2470	RES COMP 47 OHM 5P 1W
0042-2750	RES COMP 75 OHM 5P 1W
0110-2549	RES MFLM 549 OHM 1P 1/8
0110-2681	RES MFLM 68.1 OHM 1P 1/8
0110-3105	RES MFLM 105 OHM 1P 1/8W
0110-3113	RES MFLM 113 OHM 1P 1/8W
0110-3130	RES MFLM 130 OHM 1P 1/8W
0110-3243	RES MFLM 243 OHM 1P 1/8W
0110-3274	RES MFLM 274 OHM 1P 1/8W
0110-3392	RES MFLM 392 OHM 1P 1/8W
0110-3569	RES MFLM 569 OHM 1P 1/8W
0110-4110	RES MFLM 1.10 KOHM 1P 1/
0333-3100	RES VAR 100 OHM 10P 1/2W
0333-3500J	RES VAR 500 OHM 10P 1/2W
0333-6200A	RES VAR 200 KOHM 10P 1/2
1013-8315	CAP CER 150 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1014-4610	CAP CER 0.1 MFD 20P 200V
1040-7468	CAP MICA 6800 PF 1P 100V
1042-9320	CAP MICA 200 PF 5P 500V
1059-8253	CAP VAR 9-35 PF PCB MNT
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
2112-4148	DIODE GEN PURPOSE IN4148
3224-4403	TRNSTR NPN AMPLIFIER 2N4
3226-2905	TRNSTR PNP SW/AMP 2N2905
4012-74C74	IC CMOS MM74C74
4012-7404	IC TTL SN7404N PLSTC
4012-7407	IC TTL SN7407N PLSTC
4012-74123	IC TTL SN74123N PLSTC
4012-75182	IC LINEAR SN75182AN PLST

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
4760-0111	IC OPTO-COUPLER TIL111
5032-2239	INDCTR MLD 39 UH 10P
5033-2215	INDCTR MLD 15 UH 10P
5924-0256	XFMR DC ISOL TMCT2.5-6
7000-0172	RELAY 8 PIN DIP #172DIP-
9020-5762	XFMR PULSE PE-5762
9100-0112	HEAT SINK TO-5 TRNSTR 29
9111-0005	COMPONENT SPACER TO-5 LE
9601-0535	S5102TX OUTPUT AMP PCB

TABLE 5-7

PARTS LIST FOR MOTHERBOARD PRINTED CIRCUIT BOARD (P1)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-3240	RES COMP 240 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0110-2158	RES MFLM 15.8 OHM 1P 1/8
0110-3768	RES MFLM 768 OHM 1P 1/8W
0333-3500J	RES VAR 500 OHM 10P 1/2W
1013-8510E	CAP CER .01 MFD 20P 100V
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
4200-0317K	IC LINEAR REGULATOR LM31
8000-0045	SCREW PNHD MET NO.4-40X3
8000-1002	NUT HEX MET NO.4-40
8000-1202	LOCKWASHER NO.4
9313-0001	CONN EDGE DUAL 22 POS PC
9601-0534	S51C2TX MOTHER BD PCB

TABLE 5-8
PARTS LIST FOR
CHASSIS WIRING

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0012-3100	RES COMP 100 OHM 5P 1/8
0012-3110	RES COMP 110 OHM 5P 1/8
0012-4560	RES COMP 5.6 KOHM 5P 1/8
0012-5330	RES COMP 33 KOHM 5P 1/8W
8000-0116	SCREW PNHD MET NO.8-32X7
8000-1205	LOCKWASHER NO.8
8000-3200	CABLE CLAMP PLASTIC 1/8
8000-3201	CABLE CLAMP PLASTIC 3/16
8000-3202	CABLE CLAMP PLASTIC 1/4
8000-9008	CORCOM MOLEX PIN 0205120
9511-7226	S5102TX COMM F/P ASSY
9531-7238	S5102 TX CHASSIS ASSY: M
9551-7242	S5102TX COMM AC/DC HARNE
9551-7248	CABLE ASSY COAXIAL
9551-7249	CABLE ASSY COAXIAL
9551-7250	CABLE ASSY COAXIAL
9551-7251	CABLE ASSY COAXIAL
9551-7252	CABLE ASSY COAXIAL
9701-7157	S5102 PC SUPPORT BRACKET

TABLE 5-9

PARTS LIST FOR FRONT PANEL ASSEMBLY

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
2274-5353	DIODE LED YELLOW MV5353
8000-0001	SCREW PNHD MET NO.2-56X1
8000-0005	SCREW PNHD MET NC.2-56X1
8000-0045	SCREW PNHD MET NO.4-40X3
8000-0086	SCREW PNHD MET NO.6-32X7
8000-0147	SCREW PNHD MET NO.10-32X
8000-0404	WASHER FIBRE BLACK HHS 2
8000-1000	NUT HEX MET NO.2-56
8000-1200	LOCKWASHER NO.2
8000-1202	LOCKWASHER NO.4
8000-1204	LOCKWASHER NO.6
8000-1206	LOCKWASHER NO.10
8000-1509	LUG SOLDER ANGLE NO.10
8000-5002	EECO 97SG THWHL Sw HDWR
8000-5010	EECO 97SG THWHL SW.STOPS
8000-5011	EECO THWHL SW SPACER .35
9000-0002	LINE FILTER 6J4
9000-0002A	CORCOM 6J4 .125 PANEL CL
9000-0105	FUSE 3/4A SLO-BLO 3AG
9190-0002	HANDLE HHS 2052
9200-0014	SWITCH TOGGLE SPDT CK710
9200-0043	SWITCH THUMBWHL EECO 197
9203-0000	SWITCH PB MMNTRY SPST CK
9203-0008	SWITCH PB 3PDT CK8321
9203-0100	SWITCH PB DPDT 2XFA17.5
9203-0102	SWITCH PB DPDT 5XFA17.5
9205-0009	SWITCH PB POWER ON/OFF
9310-0004	PATCH JACK TYPE 310
9701-7137	SWITCH BRACKET
9701-7166	S5102TX COMM NAMEPLATE
9701-7227	S5102TX COMM F/P FINISHE
9721-7138	310 MOUNTING BLOCK

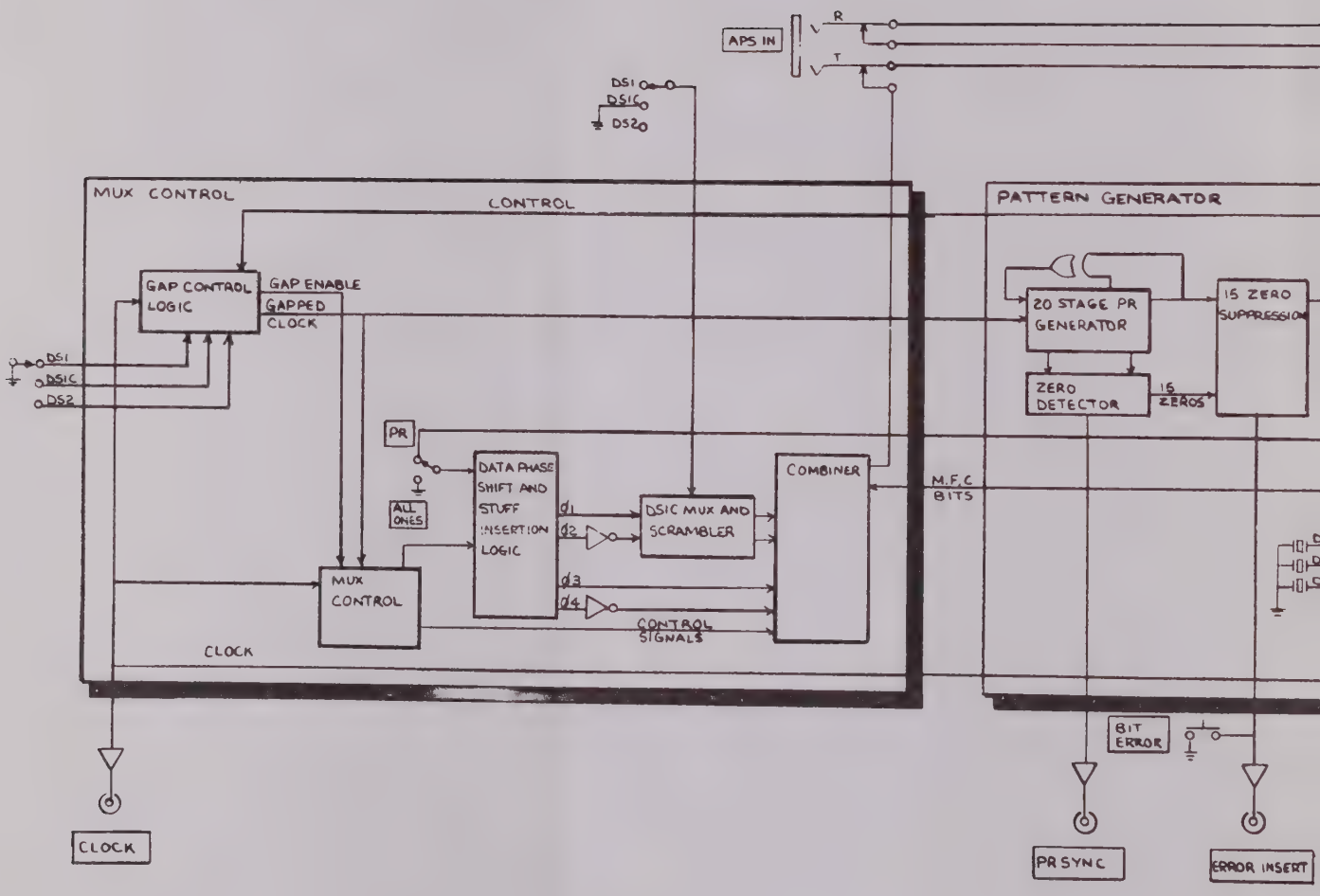
SECTION 6
DIAGRAMS

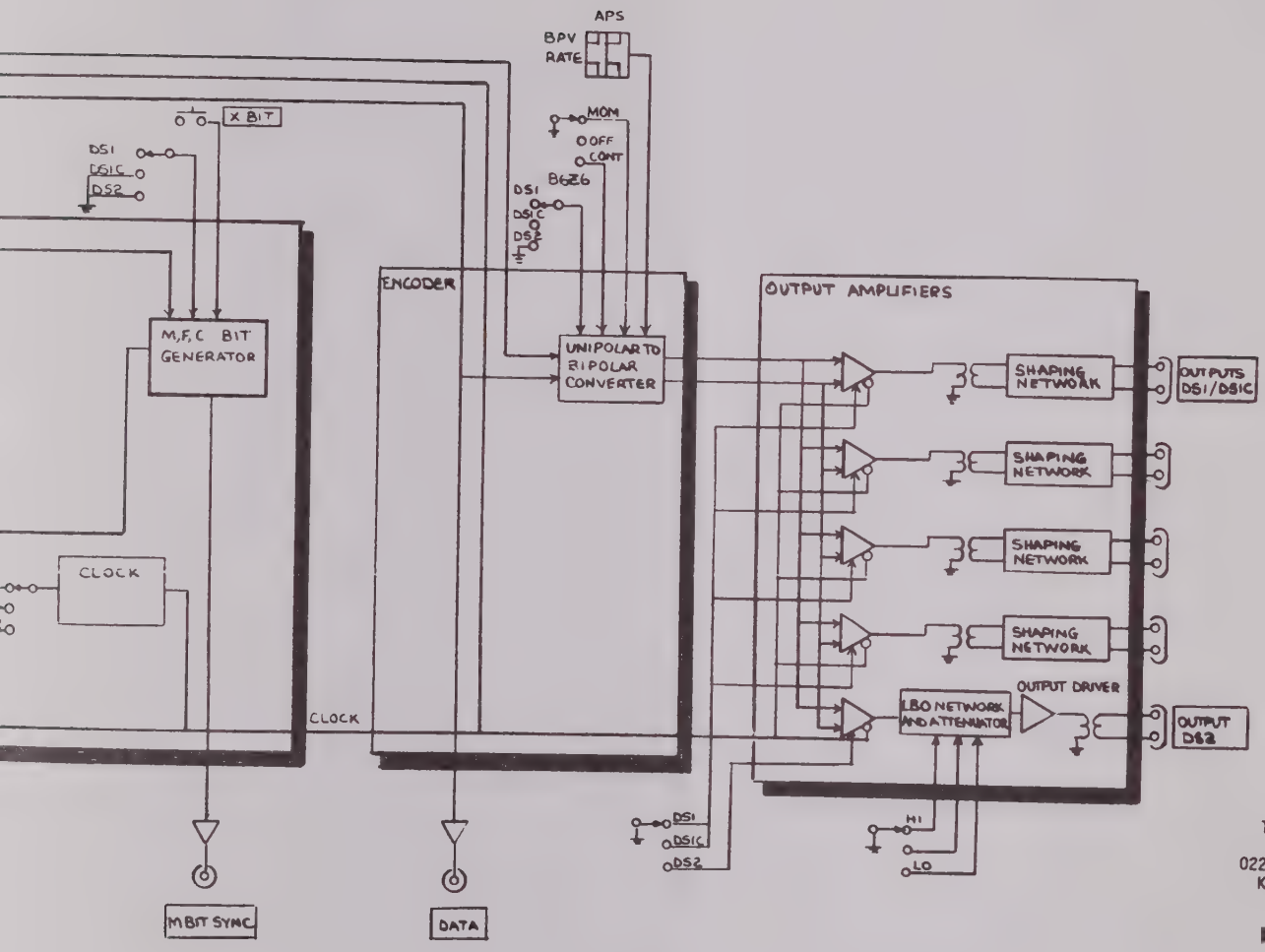
GENERAL

THIS SECTION CONTAINS THE SCHEMATIC DIAGRAMS AND COMPONENT LOCATION DIAGRAMS FOR THE S5102 ERROR RATE TEST SET (TRANSMITTER). TABLE 6-1, SHOWN ON THE FOLLOWING PAGE, IS AN INDEX OF THE ILLUSTRATIONS THAT APPEAR IN THIS SECTION.

TABLE 6-1
INDEX OF FIGURES

FIGURE	TITLE
6-1	FUNCTIONAL BLOCK DIAGRAM
6-2	PATTERN GENERATOR LOADING DRAWING AND SCHEMATIC.
6-3	MUX CONTROL ASSEMBLY DIAGRAM AND SCHEMATIC.
6-4	ENCODER AND ERROR CONTROL ASSEMBLY DIAGRAM AND SCHEMATIC.
6-5	OUTPUT AMPLIFIER LOADING DIAGRAM AND SCHEMATIC.
6-6	MOTHERBOARD LOADING DIAGRAM, SCHEMATIC, AND WIRING DIAGRAM.
6-7	FRONT-PANEL WIRING DIAGRAM.
6-8	CHASSIS WIRING DIAGRAM.


APS IN
R
T
DS1
DS1C
DS2
MUX CONTROL
CONTROL
GAP CONTROL LOGIC
GAP ENABLE
GAPPED CLOCK
DS1
DS1C
DS2
PR
ALL ONES
DATA PHASE SHIFT AND STUFF INSERTION LOGIC
ϕ1
ϕ2
ϕ3
ϕ4
DSIC MUX AND SCRAMBLER
COMBINER
MUX CONTROL
CONTROL SIGNALS
CLOCK
M.F.C BITS
PATTERN GENERATOR
20 STAGE PR GENERATOR
ZERO DETECTOR
15 ZEROS
15 ZERO SUPPRESSION
BIT ERROR
CLOCK
PR SYNC
ERROR INSERT



Tau-Tron
form
0221-0382C
KS-22331
1 of 1

BLOCK

Fig. 6-1

PC 2
53102
ASSY TDK-17123
REV
PATTERN
GENERATOR
SEE NOTE 2
PC PIN
CONCORD
10-916-2-04
74LS175
74L530
74LS175
74LS30
14013*
14017*
74LS175
74L502
74LS175
14027*
14001*
74LS175
74L530
74L500
14027*
14012*
19512*
74L586
74L504
74LS175
14011*
14023*
74LS123
75182
75182
74LS10
74LS74
74L586
74L502
14027*
74L505
74LS04
74LS10
74L500
7416
14049*
14001*
19512*
TT0533E
10K
10K
10K
9.1K
COMPONENT SIDE

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REV PER PDC# 00544 RFP	10-19-79	[illegible]
	B	REV PER DCN 00604	11-Jan-80	C.S.
	C	CHANGED R41,42,72,77 FROM 2.2Ω TO 1.5Ω; CHANGED C23,24,28 & 29 TO 1.5Ω	9-18-80	A.B.M.
	D	REV PER DCN 00714 C.A.	9-2-80	[illegible]
	E	REV PER DCN 00774 11-10-80 C.S.	12-12-80	[illegible]
	F	REV PER DCN 00866 SJ 341-81	5-22-87	[illegible]
	G	REV PER ECO#1371 BAB 4-483	4-7-87	[illegible]

SEE DETAIL A

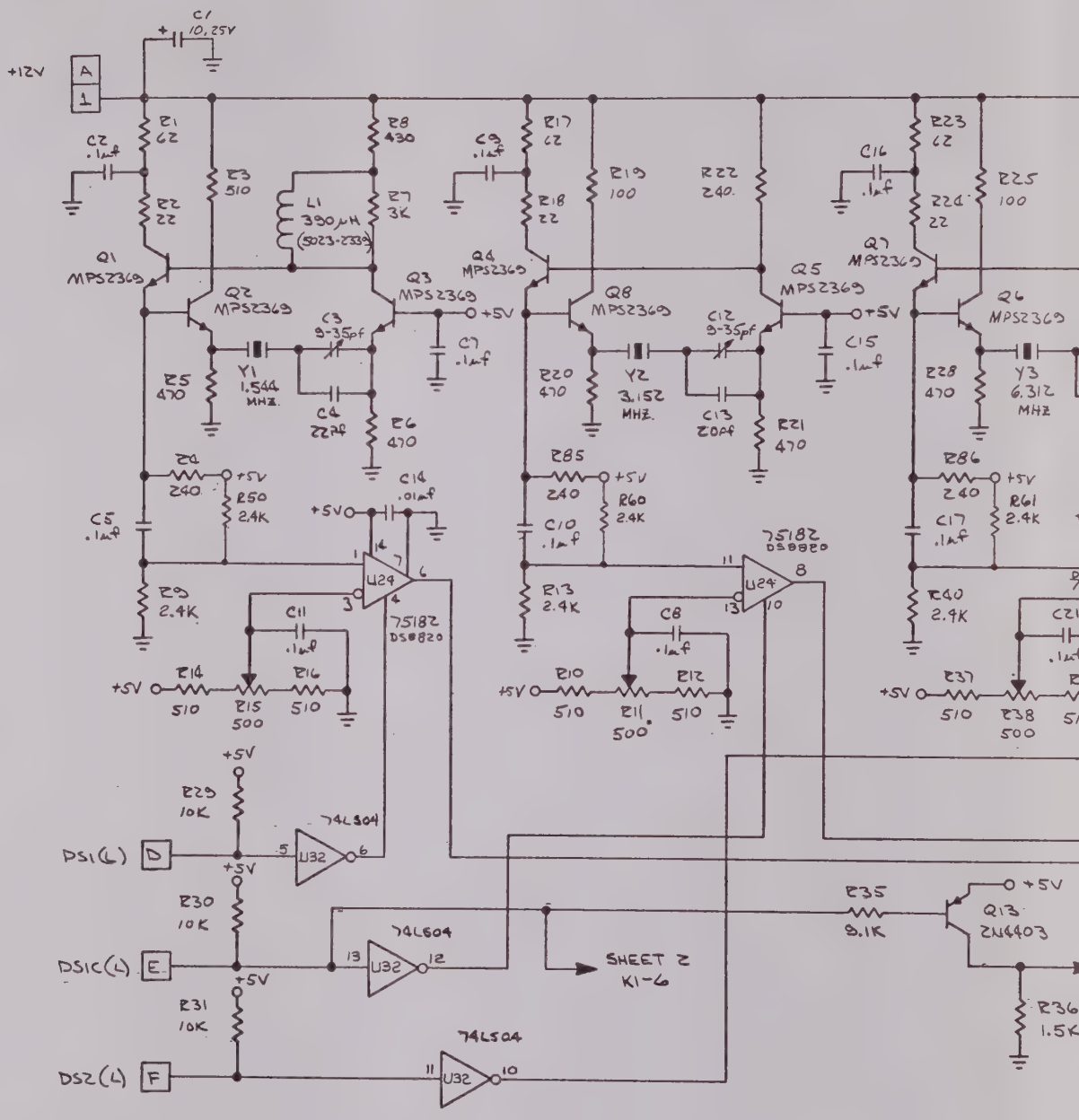
DETAIL A
MOUNT AS SHOWN

NOTES:

1. UNLESS OTHERWISE SPECIFIED.
   a) RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5%.
   b) CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSY IN THE DESIGNATED AREA.
3. * - DENOTES STATIC SENSITIVE DEVICE.

Fig. 6-2
1 of 3

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO.	tau-tron INC Chelmsford, MA 01824
	TOLERANCES: ANGLES ±	DR R. Rentas 10-19-79	
	FRACTIONS ±	CHK R. MONTEIRO 10-14-79	DRAWING TITLE
	3 PLACE DECIMALS ±	APPD W. Little 11-8-79	AMTR PATTERN GENERTOR LOADING DRAWING
	2 PLACE DECIMALS ±		
	1 PLACE DECIMALS ±		
	MATERIAL:		
55102 Tx		APPROVED	SIZE D / CODE IDENT NO. / DRAWING NO. TDK-47123-1 / REV G
NEXT ASSY / USED ON		BY DIRECTION OF	SCALE 2/1 / 55102 / SHEET 1 OF 3
APPLICATION			



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
   B) CAPACITANCE VALUES ARE IN MICROFARADS.
2. □ DENOTES EDGE CONNECTOR PIN NO. OR LETTER.
3. * VALUES TO BE DETERMINED IN TEST.
4. C37 - C42 ARE .01uf DECOUPLING CAPACITORS

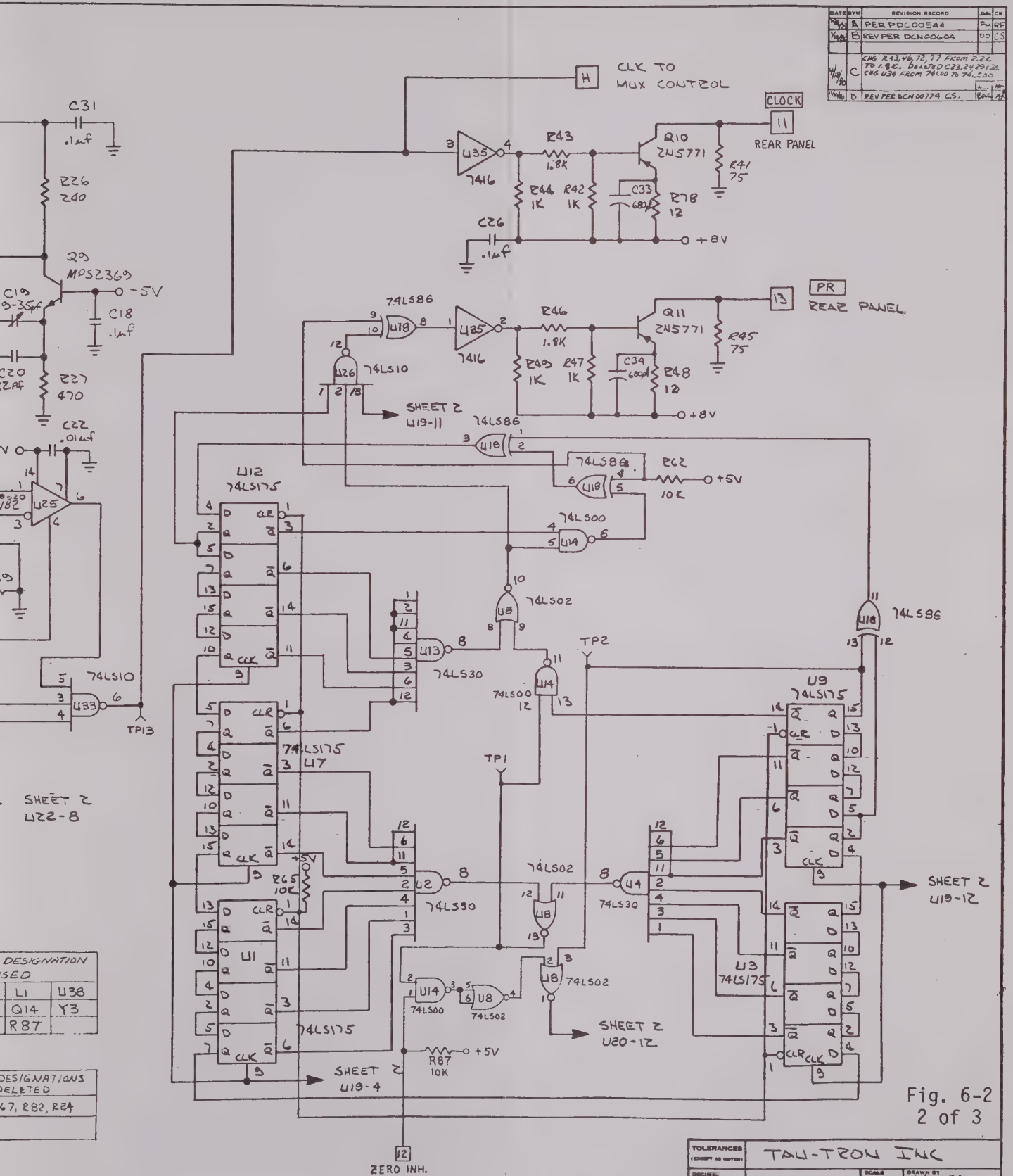
LAST

C42
CR1
K1

REF.

R66,
C28

BRUNING 40-21



DESIGNATION USED			
	L1	U38	
	Q14	Y3	
	R87		

DESIGNATIONS DELETED
47, R82, R84

DATE	BY	REVISION RECORD	DR.	CK
12/7/78	A	PER PDC00544	FM	RF
1/16/79	B	REV PER DCN00604	DD	CS
4/16/80	C	CHG R43,46,72,77 FROM 2.2K TO 1.8K. DELETED C23,24,29,32. CHG U36 FROM 74L00 TO 74LS00		
10/16/80	D	REV PER DCN 00774 C.S.	BAC	MP

Fig. 6-2
2 of 3

TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC		
DECIMAL ± .XX	S5102 TRANSMITTER	SCALE .XX	DRAWN BY W. HESS
FRACTIONAL ± .XX	TITLE PATTERN GENERATOR, SCHEMATIC		APPROVED BY BUDD
ANGULAR ± .X°	DATE 5/3/79	DRAWING NUMBER TDJ-17124	REV D

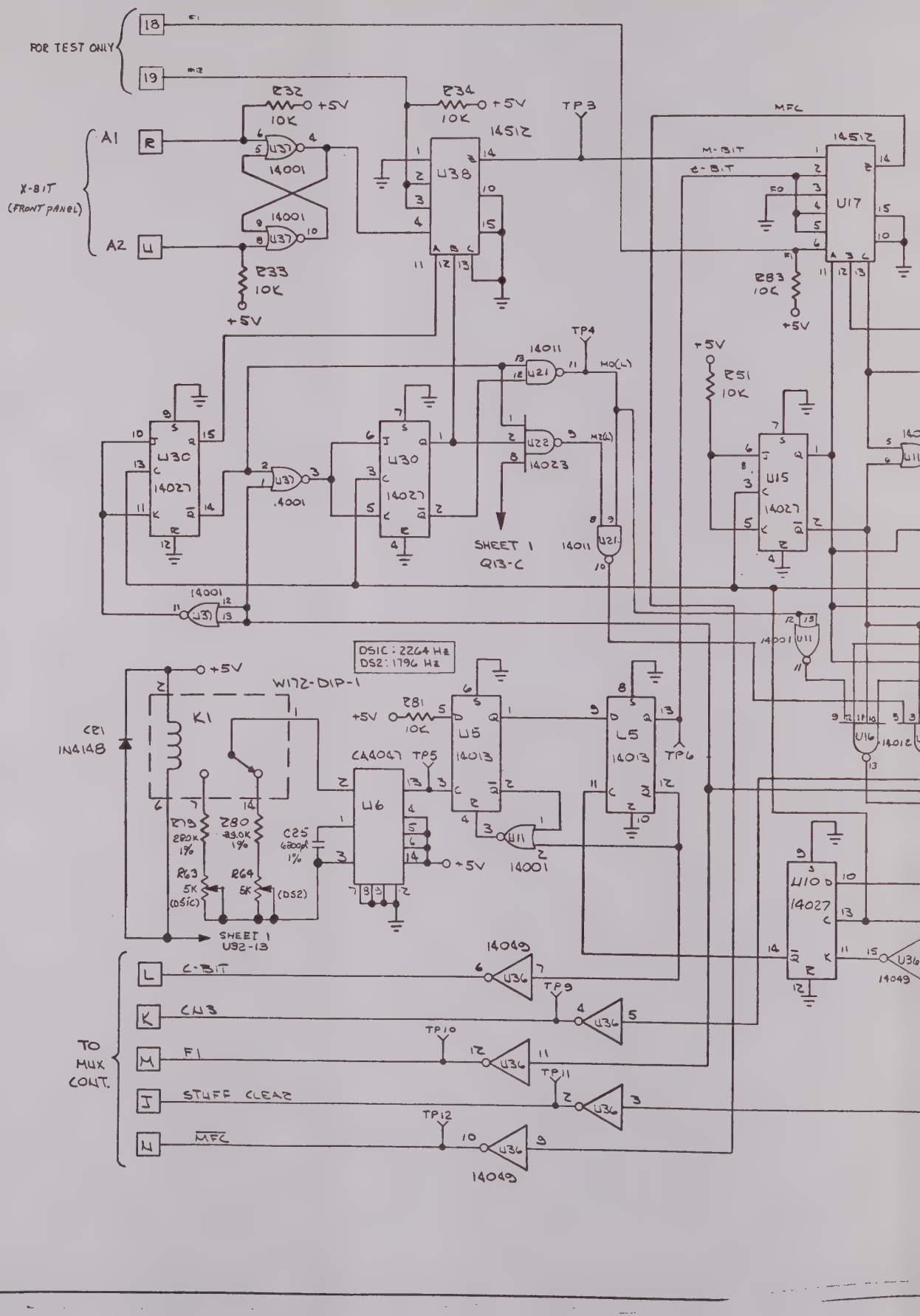

FOR TEST ONLY
18
19
X-BIT (FRONT PANEL)
A1
A2
R
U
R32 10K +5V
R34 10K +5V
R33 10K +5V
14001
14512
U38
TP3
MFC
M-BIT
C-BIT
U17
R83 10K +5V
14011
U21
TP4
MO(L)
U30
14027
U37
U22
14023
MZ(L)
SHEET 1 Q13-C
R51 10K +5V
U15
DS1C: 2264 Hz
DS2: 1796 Hz
W172-DIP-1
K1
CR1 IN4148
R81 10K +5V
U5
14013
CA4047
U6
TP5
TP6
R79 280K 1%
R80 33.0K 1%
R63 5K (DS1C)
R64 5K (DS2)
C25 6800pf 1%
U11
U16
14012
U10
14027
SHEET 1 U32-13
TO MUX CONT.
L C-BIT
K CW3
M F1
J STUFF CLEAR
N MFC
U36
14049
TP9
TP10
TP11
TP12

Fig. 6-2
3 of 3

TOLERANCES (EXCEPT AS NOTED)	TAU TRON INC
DECIMAL ±	SS102 TRANSMITTER
FRACTIONAL ±	TITLE: PATTERN GENERATOR, SCHEMATIC
ANGULAR ±	DATE: 5/9/79
SCALE	DRAWN BY: W. HUBSCHMAN
APPROVED BY	BDD
DRAWING NUMBER	TDJ-17124
REV	D

MUX CONTROL

ASSY TCK-17120 REV

R10 10K

C18 .01

74LS74 U1

74LS08 U2

74LS02 U3

74LS00 U4

C11 .01

R11 1K

74LS20 U10

74LS00 U11

74LS01 U12

74LS162 U13

C9 .01

R9 10K

74LS10 U19

74LS00 U20

74LS112 U21

74LS04 U22

PIN TP7

PIN TP6

C1 .01

7404 U28

74LS175 U29

74LS175 U30

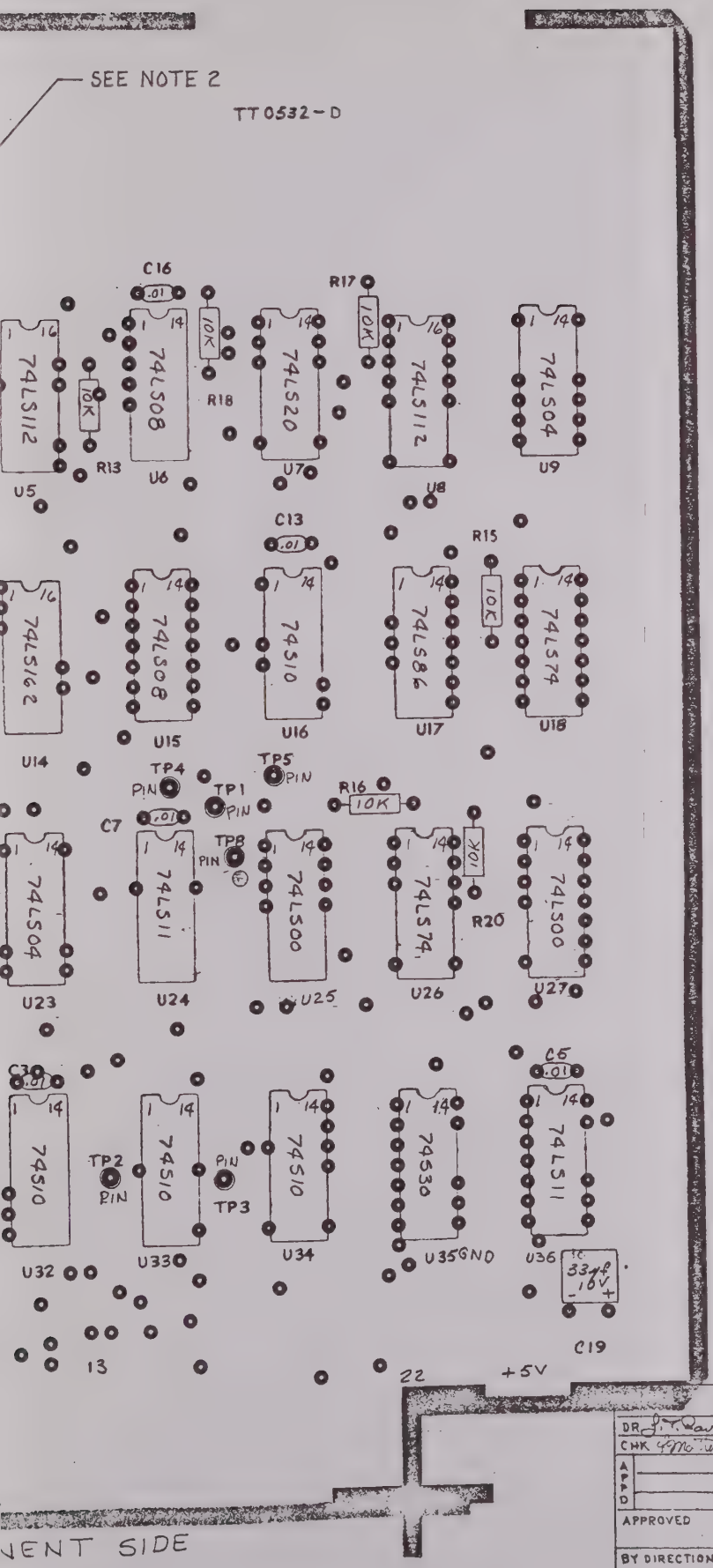
74LS175 U31

RP1 10K

GND

COMPO

REVISION RECORD				
DATE	SYM	DESCRIPTION	DR	APPROVED
4/4/79	1	UPDATED PROTOTYPE	BUDD	
8/3/79	A	RELEASED TO PRODUCTION	-	W.E.D.
8/20/79	B	RELEASED TO PRODUC. PER PDC00544	J. RAO	TM
	C	REV. PER DCN#00C04 RB		J.F.T.
19/11/80	D	REV PER DCN 00757 C.S.	11/24/80	EAC WEJ



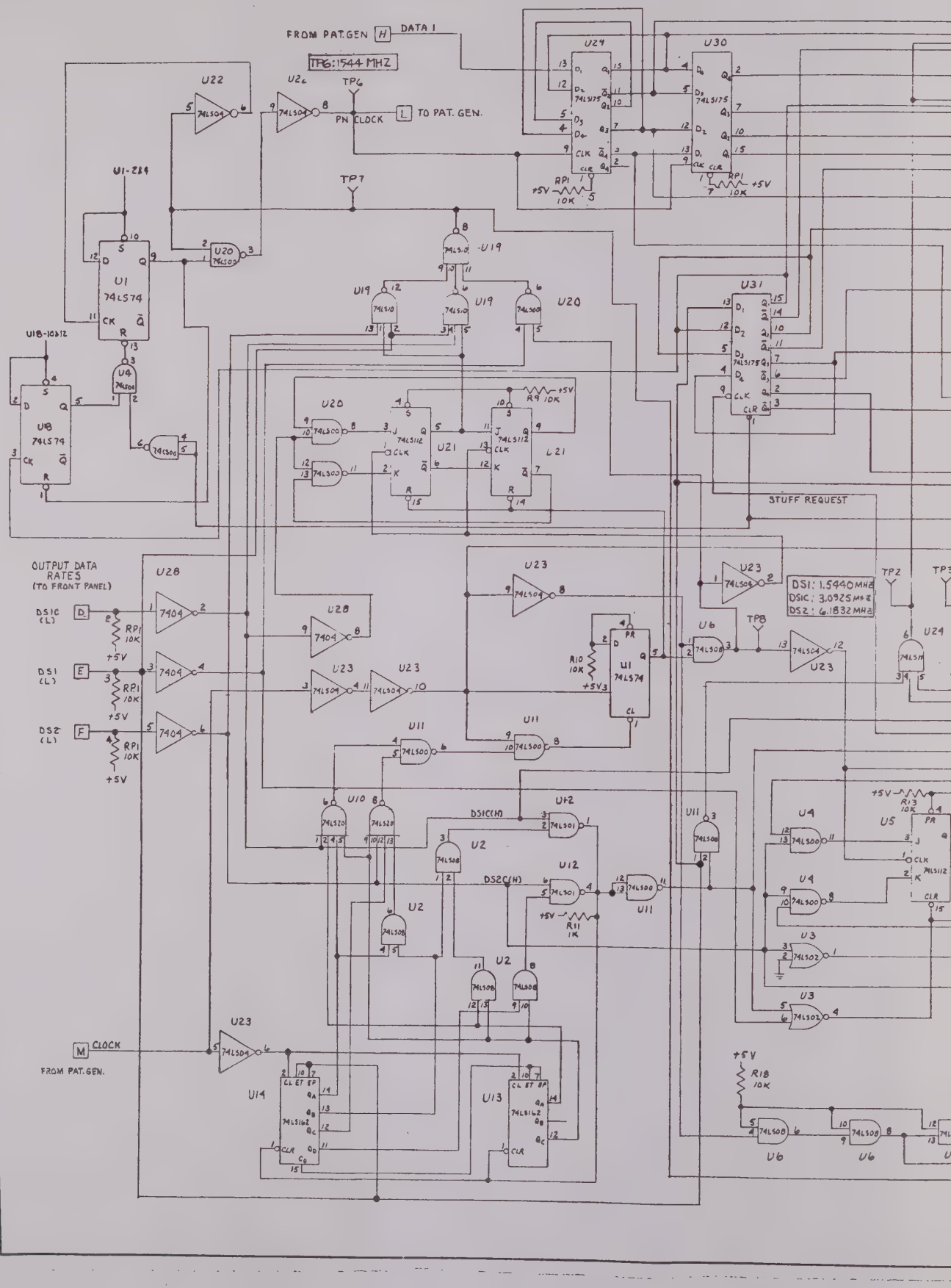
NOTES:

1. UNLESS OTHERWISE SPECIFIED
   a). RESISTANCE VALUES ARE IN OHMS 1/4W, ±5%
   b) CAPACITANCE VALUES ARE IN MICROFARADS
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA.

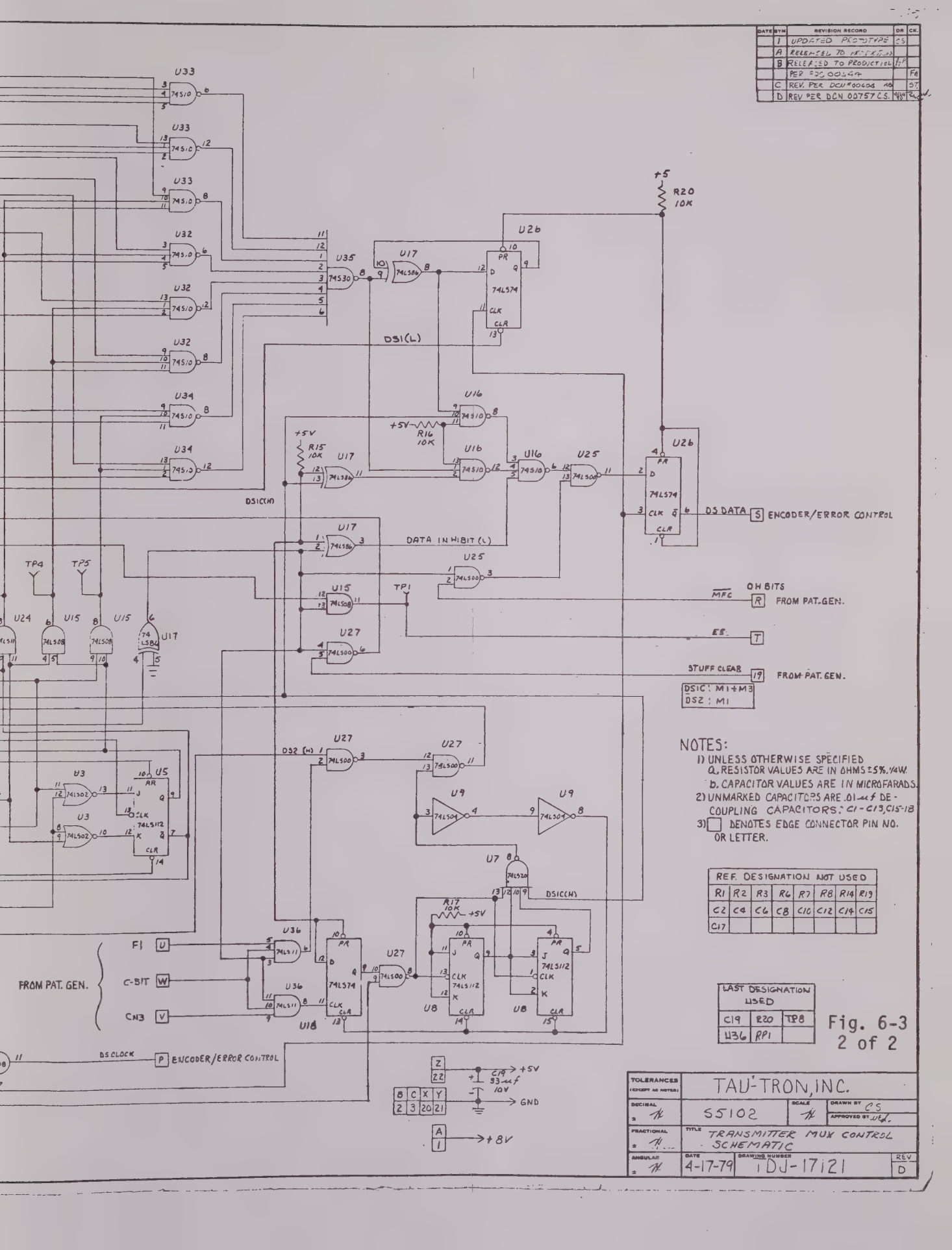
Fig. 6-3
1 of 2

DR J.T. Rao	8/27/79	tau-tron inc Chelmsford, MA. 01824
CHK TM	8/30/79	DRAWING TITLE TRANSMITTER MUX CONTROL ASS'Y DIAGRAM
APPD		
APPROVED		SIZE C | CODE IDENT NO. | DRAWING NO. TCK 17120 | REV D
BY DIRECTION OF		SCALE 2/1 | 55102 | SHEET

NENT SIDE



BRUNING 40-21



NOTES:

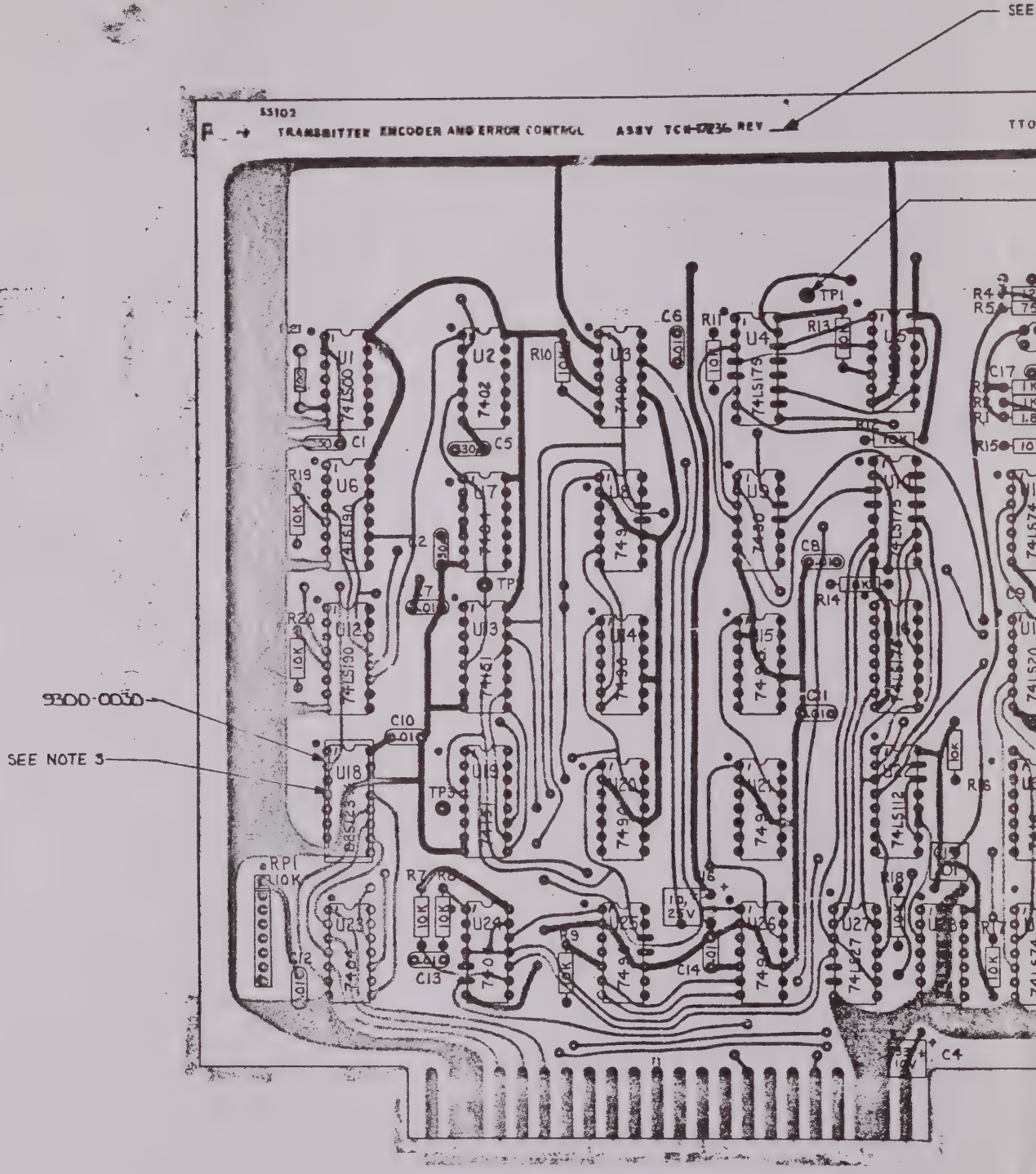
1) UNLESS OTHERWISE SPECIFIED
   a. RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
   b. CAPACITOR VALUES ARE IN MICROFARADS.
2) UNMARKED CAPACITORS ARE .01 uf DE-COUPLING CAPACITORS: C1-C13, C15-18
3) ☐ DENOTES EDGE CONNECTOR PIN NO. OR LETTER.

REF. DESIGNATION NOT USED							
R1	R2	R3	R6	R7	R8	R14	R19
C2	C4	C6	C8	C10	C12	C14	C15
C17							

LAST DESIGNATION USED		
C19	R20	TP8
U36	RP1	

Fig. 6-3
2 of 2

TOLERANCES (EXCEPT AS NOTED)	TAU-TRON, INC.
DECIMAL ± .X	55102
SCALE .X	DRAWN BY CS
FRACTIONAL ± .X	APPROVED BY
ANGULAR ± .X	TITLE: TRANSMITTER MUX CONTROL SCHEMATIC
DATE 4-17-79	DRAWING NUMBER 1DJ-17121 REV D


SEE
55102
TRANSMITTER ENCODER AND ERROR CONTROL ASSY TCM-0236 REV
TP1
9300-0030
SEE NOTE 3
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
C1
C4
C5
C6
C8
C9
C10
C11
C12
C13
C14
C17
R4
R5
R6
R7
R8
R10
R11
R13
R14
R15
R18
R19
R20
RP1
TP3
TP4
74LS00
7402
7400
74LS175
74LS174
74LS112
74LS27
74LS20
74LS190
74LS191
74LS151
74LS123
7410
7408
10K
.01
.33
39
1K
10 25V

	A	RELEASED PER DCN 00818 C.S. 1-5-81	1-8-81	[illegible]
	B	REV. PER ECO/00956 [illegible] 4 SEP 81	9-17-81	[illegible]
	C	REV PER ECO/01073 R.Vinson 1-12-82	1-13-82	[illegible]
	D	REV PER ECO-0125 R.Vinson 6-8-82	7-8-82	[illegible]

OTE 2.

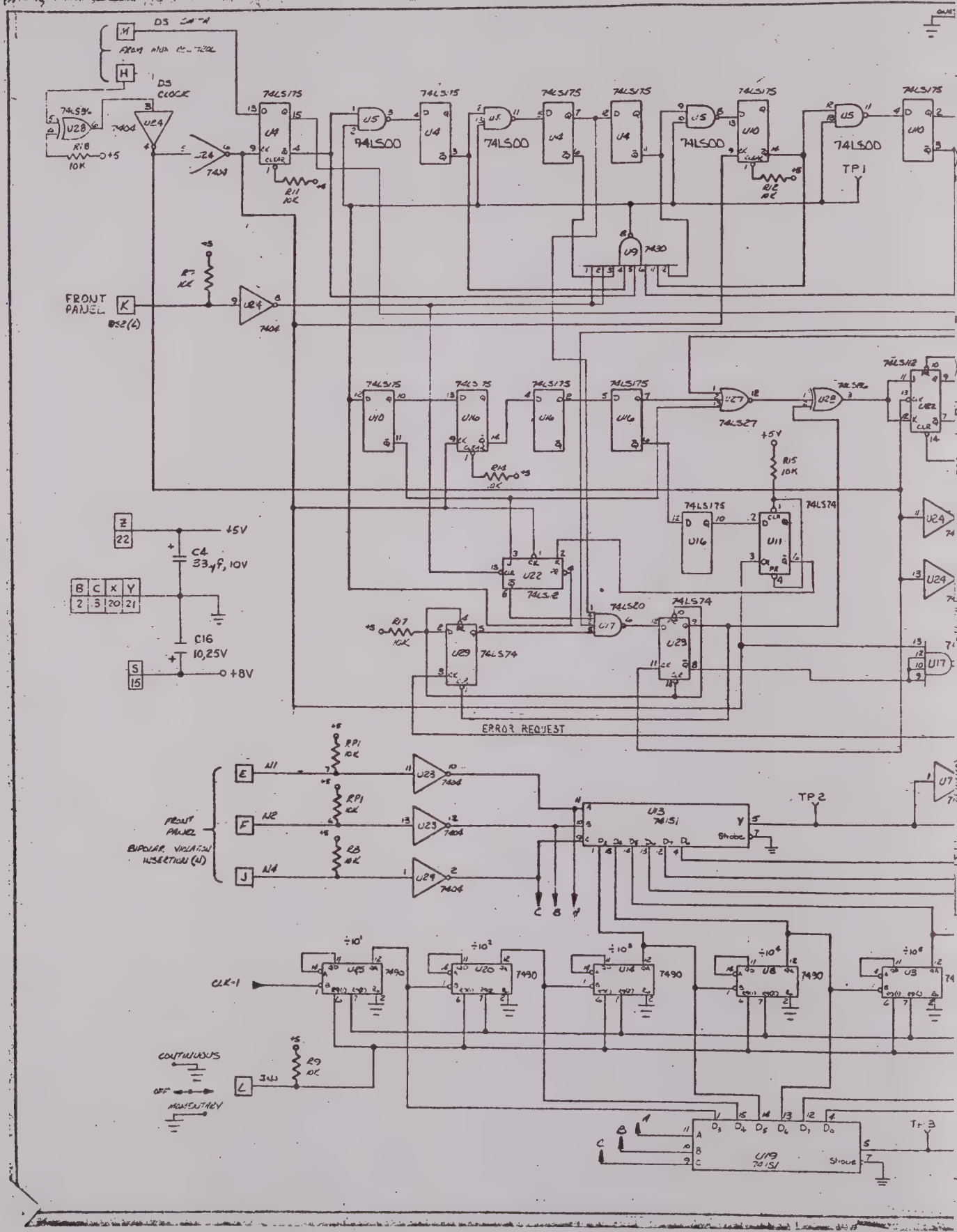
CONCORD PIN
3 PLACES TP1,2,3

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTOR VALUES ARE IN OHMS, ¼W, ±5%.
   B. CAPACITOR VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA.
3. * DENOTES STATIC SENSITIVE DEVICE.

Fig. 6-4
1 of 2

	C. Smith 1-5-81	tau-tron
	B. Cooper 1-8-81	ASSEMBLY, ENCODER & ERROR CONTROL PCB (TT0529) (COMMERCIAL)
TEK-17155 S5102 TX	APPROVED	D / TDK-17236 / D
		S5102 TX SHEET OF


DS CLOCK
74LS175
74LS00
74LS27
74LS374
74LS20
74LS112
7404
7430
7490
74151
FRONT PANEL
BIPOLAR VIOLATION INSERTION (N)
ERROR REQUEST
CLK-1
CONTINUOUS
MOMENTARY
+5V
+8V
TP1
TP2
TP3

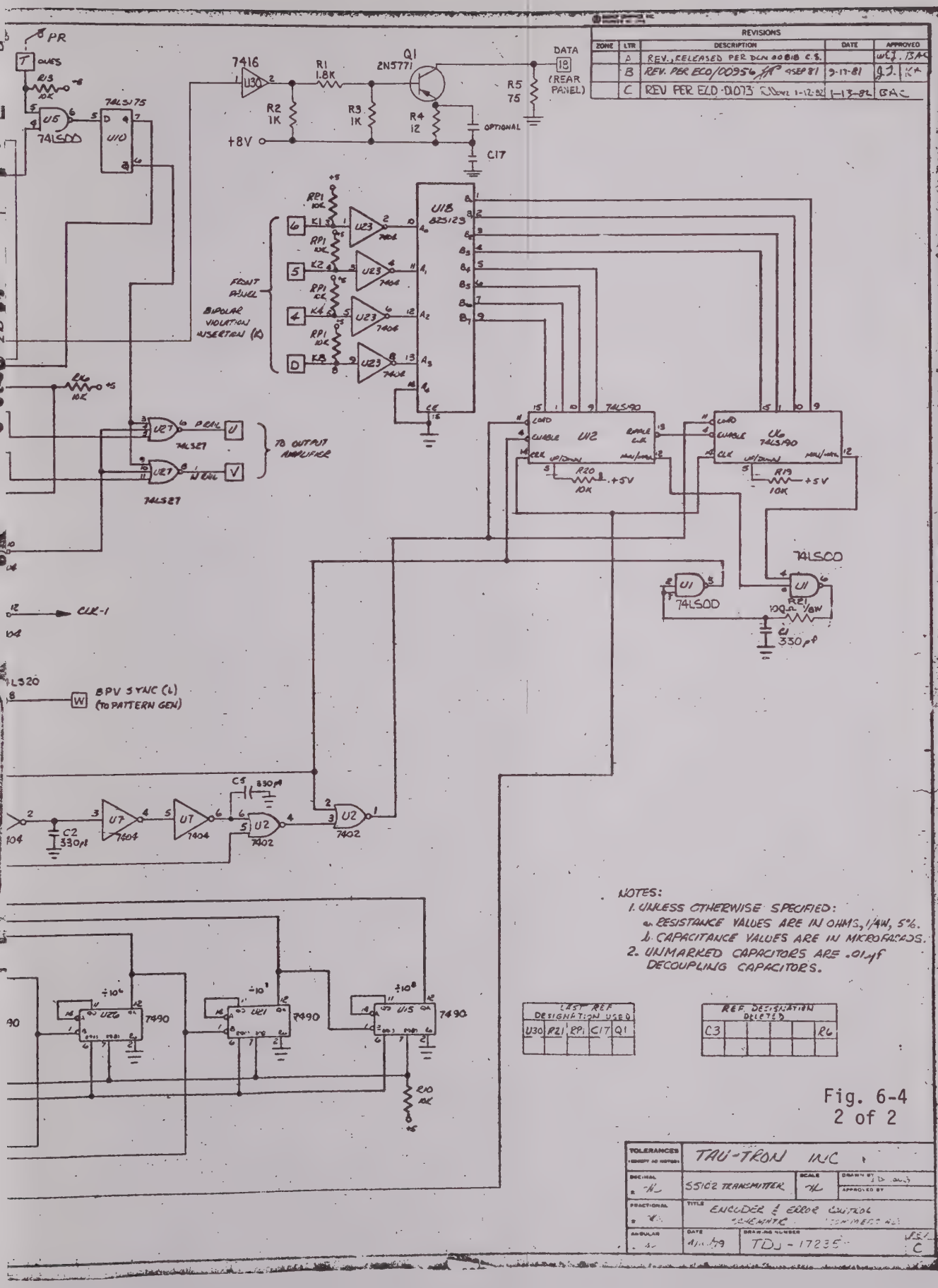
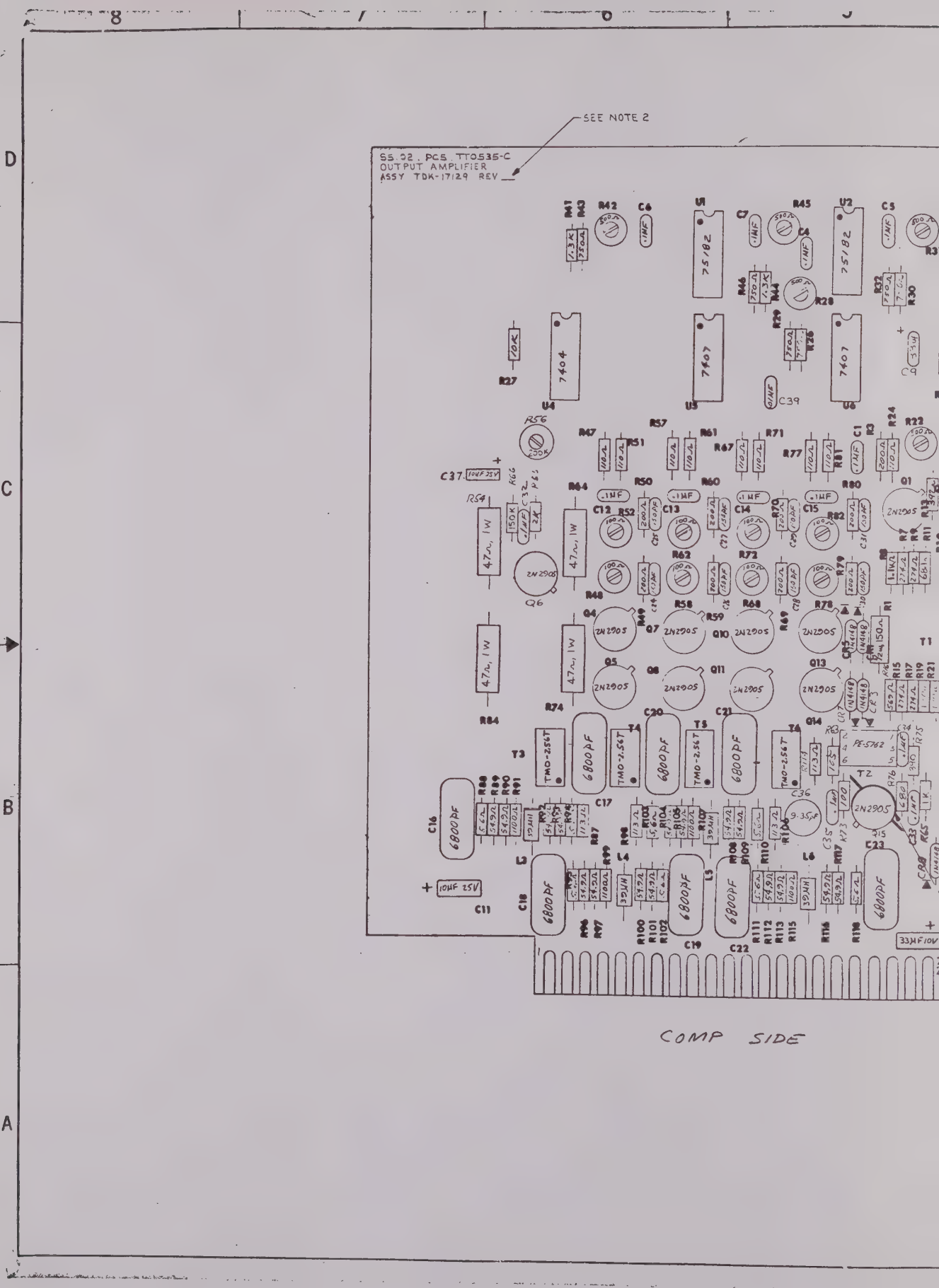
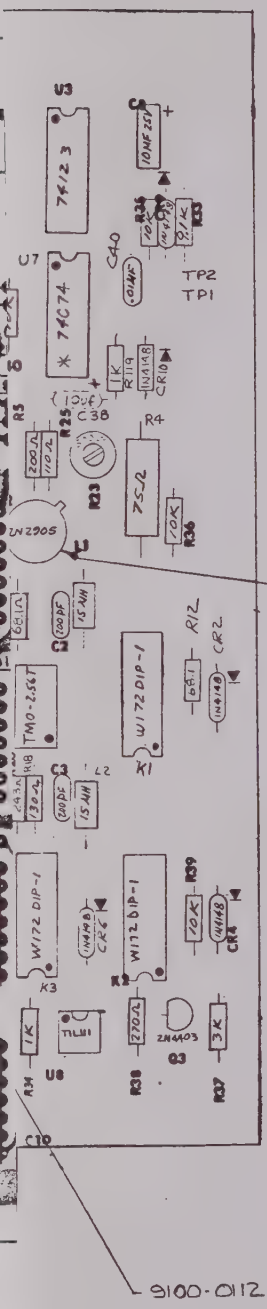

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REV., RELEASED PER DCN 80818 C.S. | | WCJ. BAC
B | REV. PER ECO/00956 | 9-17-81 | GJ. KA
C | REV PER ECO 01073 | 1-13-82 | BAC
7416
R1 1.8K
Q1 2N5771
DATA 18 (REAR PANEL)
R5 75
R2 1K
R3 1K
R4 12
OPTIONAL
C17
+8V
74LS175
74LS00
U18 82S123
FRONT PANEL
BIPOLAR VIOLATION INSERTION (K)
74LS27
TO OUTPUT AMPLIFIER
74LS90
R20 10K
R19 10K
+5V
74LS00
R21 100Ω 1/8W
C1 330pF
CLK-1
BPV SYNC (L) (TO PATTERN GEN)
C5 330pF
C2 330pf
7404
7402
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
b. CAPACITANCE VALUES ARE IN MICROFARADS.
2. UNMARKED CAPACITORS ARE .01μf DECOUPLING CAPACITORS.
LAST REF DESIGNATION USED
U30 | R21 | RP1 | C17 | Q1
REF. DESIGNATION DELETED
C3 | R4
7490
R10 10K
TOLERANCES
TAU-TRON INC.
SSIC2 TRANSMITTER
SCALE NL
TITLE ENCODER & ERROR CONTROL SCHEMATIC
DRAWING NUMBER TDJ - 17235
REV C

Fig. 6-4
2 of 2


SEE NOTE 2
SS.02 . PCS TT0535-C
OUTPUT AMPLIFIER
ASSY TDK-17129 REV
COMP SIDE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION PER PDC 00544	11/23/77	MLK
	B	REV PER DCN 00620 RAL	2/12/80	RL
	C	REV PER DCN 00743 CA	9-23-80	[illegible]
	D	REV PER DCN 00836 JJ	4-22-81	[illegible]
	E	REV PER ECO 00902 JJ	5-12-81	C.S. AFM
	F	REV PER ECO#01032 C.S.	11-2-81	[illegible]
	G	REV PER ECO#01056 JJ	11-20-81	RL

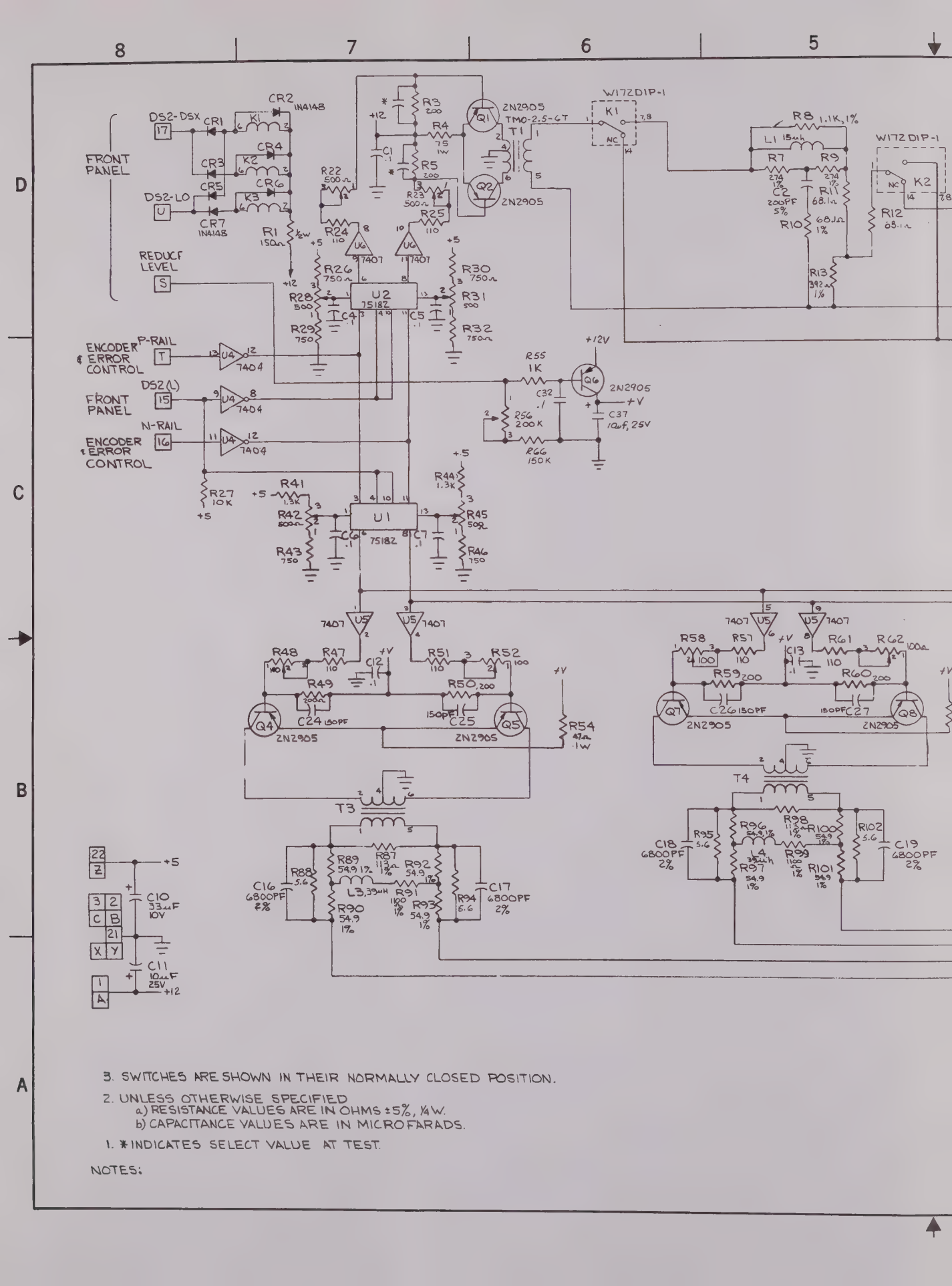


NOTE:
1. TRANSISTOR PADS REQUIRED FOR ALL 2N2905
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSY IN THE DESIGNATED AREA.
3. * DENOTES STATIC SENSITIVE DEVICE.

Fig. 6-5
1 of 2

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO. DR L.FRANEK 11-26-79 CHK R.A. Tinsley 11/28/79 APPD Wd Hite 12/3/79 APPROVED BY DIRECTION OF	tau-tron INC Chelmsford, MA 01824 DRAWING TITLE LOADING DIAGRAM OUTPUT AMPLIFIER

TDK-17126	55102 TX	SIZE D	CODE IDENT NO.	DRAWING NO. TDK-17129 REV G
NEXT ASSY	USED ON	SCALE 2:1	55102 TX	SHEET 1 OF 2
APPLICATION				



3. SWITCHES ARE SHOWN IN THEIR NORMALLY CLOSED POSITION.

2. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE VALUES ARE IN OHMS ±5%, ¼W.
   b) CAPACITANCE VALUES ARE IN MICROFARADS.

1. *INDICATES SELECT VALUE AT TEST.

NOTES:

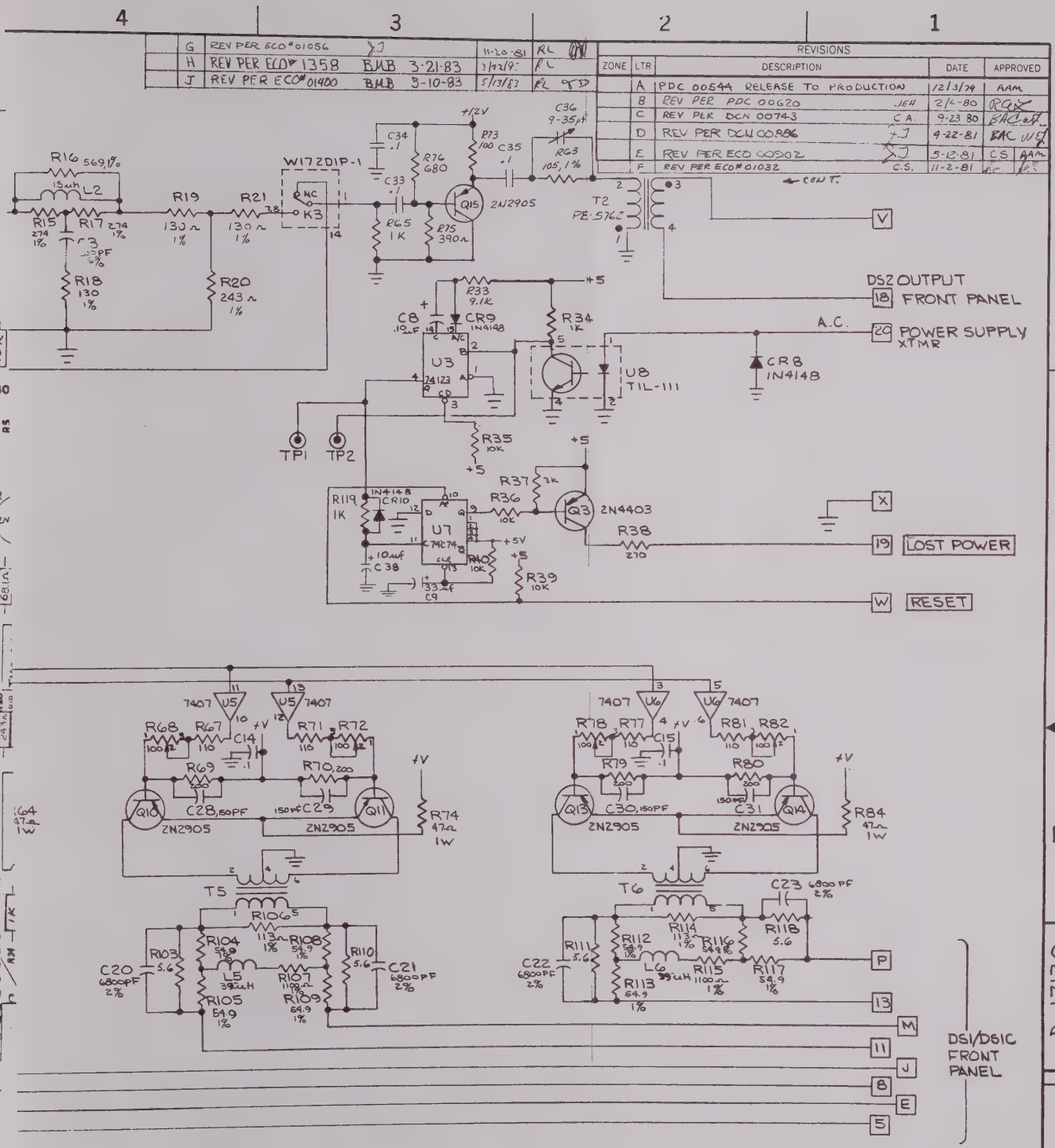
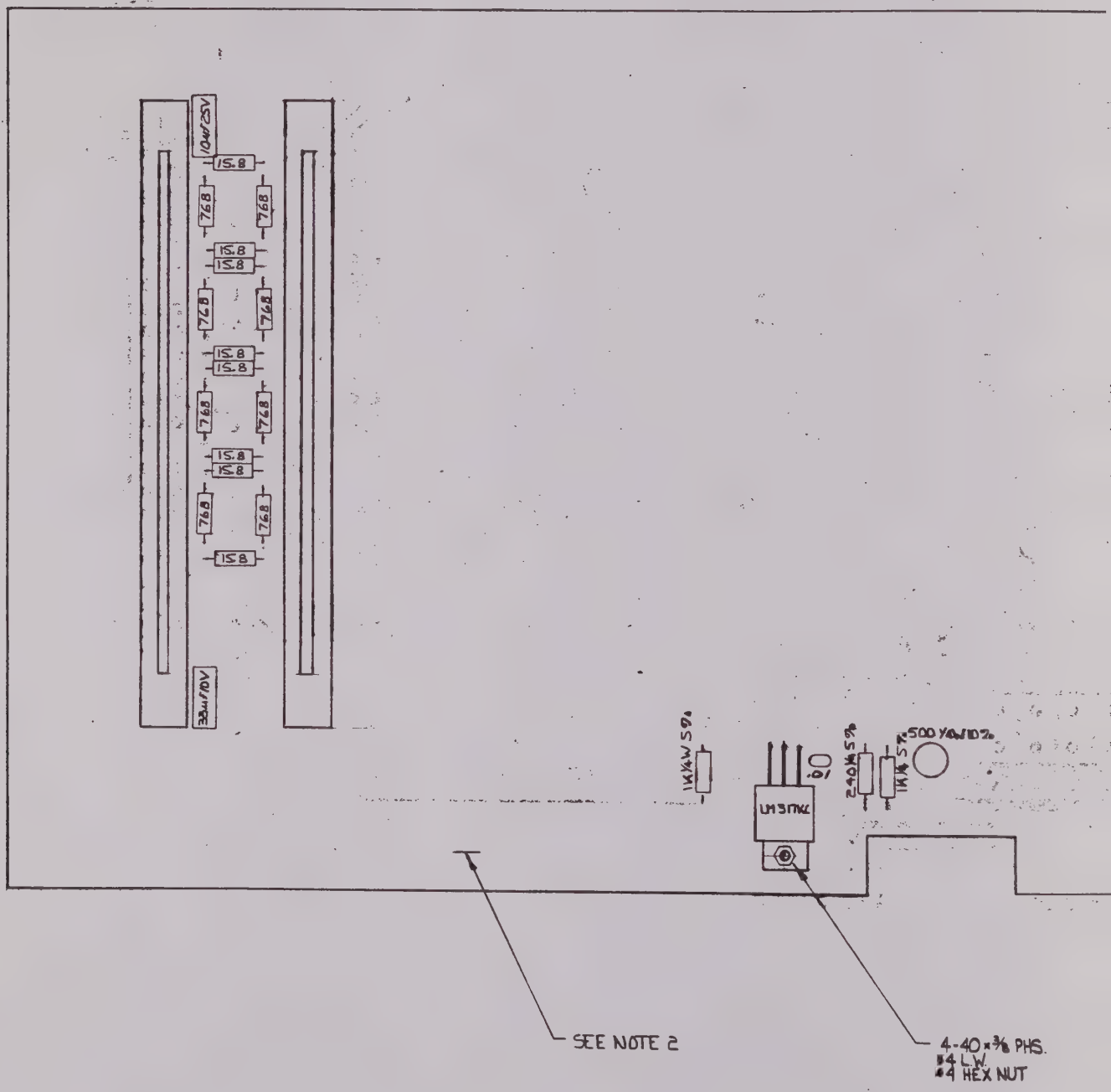
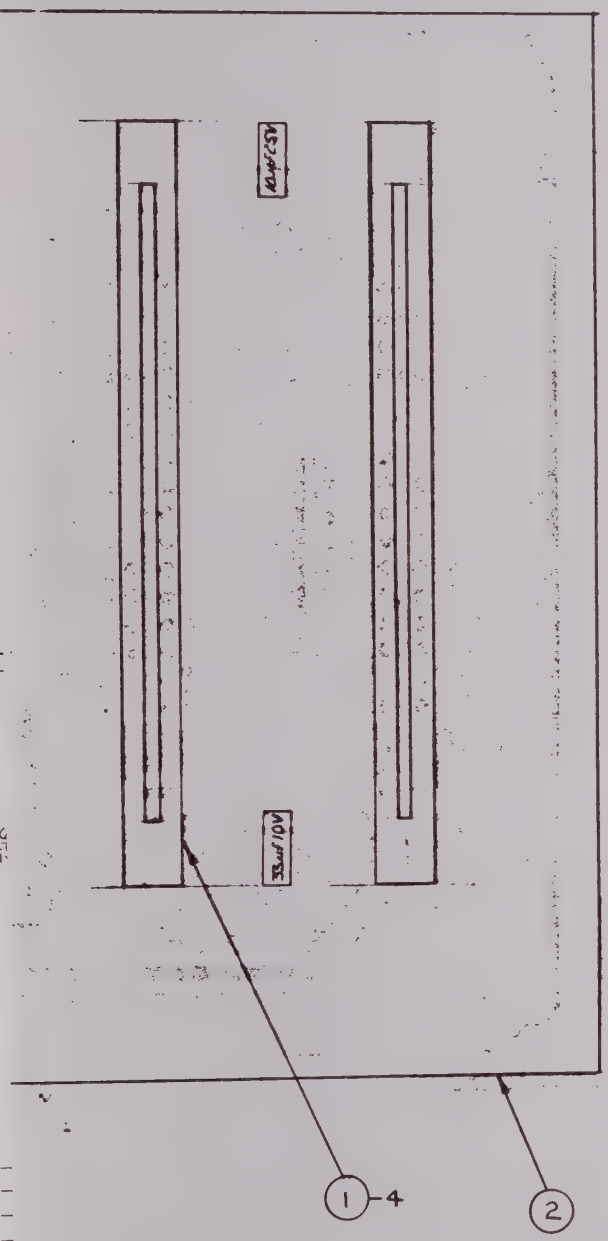


Fig. 6-5
2 of 2

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.	tau-tron inc Chelmsford, Mass. 01824
		DR D. OLIVER 29NOV79	DRAWING TITLE OUTPUT AMPLIFIER SCHEMATIC
		CHK T. SEIZER 3-DEC79	
		APPD WEK 10-10-80	
S5102TX		APPROVED	SIZE D · CODE IDENT NO. · DRAWING NO. D-17130 · REV J
NEXT ASSY · USED ON		BY DIRECTION OF	SCALE 4/1 · S5102 TX · SHEET 1 OF
APPLICATION			


10uF/25V
15.8
768
15.8
15.8
768
768
15.8
15.8
768
768
15.8
15.8
768
768
15.8
768
768
15.8
33uF/10V
1K/4W 5%
.01
LM317MKT
240Ω 5%
1K 5%
500 Ω W/10 Turn
SEE NOTE 2
4-40 x 3/8 PHS.
#4 LW
#4 HEX NUT

	H	REDRAWN PER ECO-01156 R.Nunez	1-9-82	RL



NOTES:

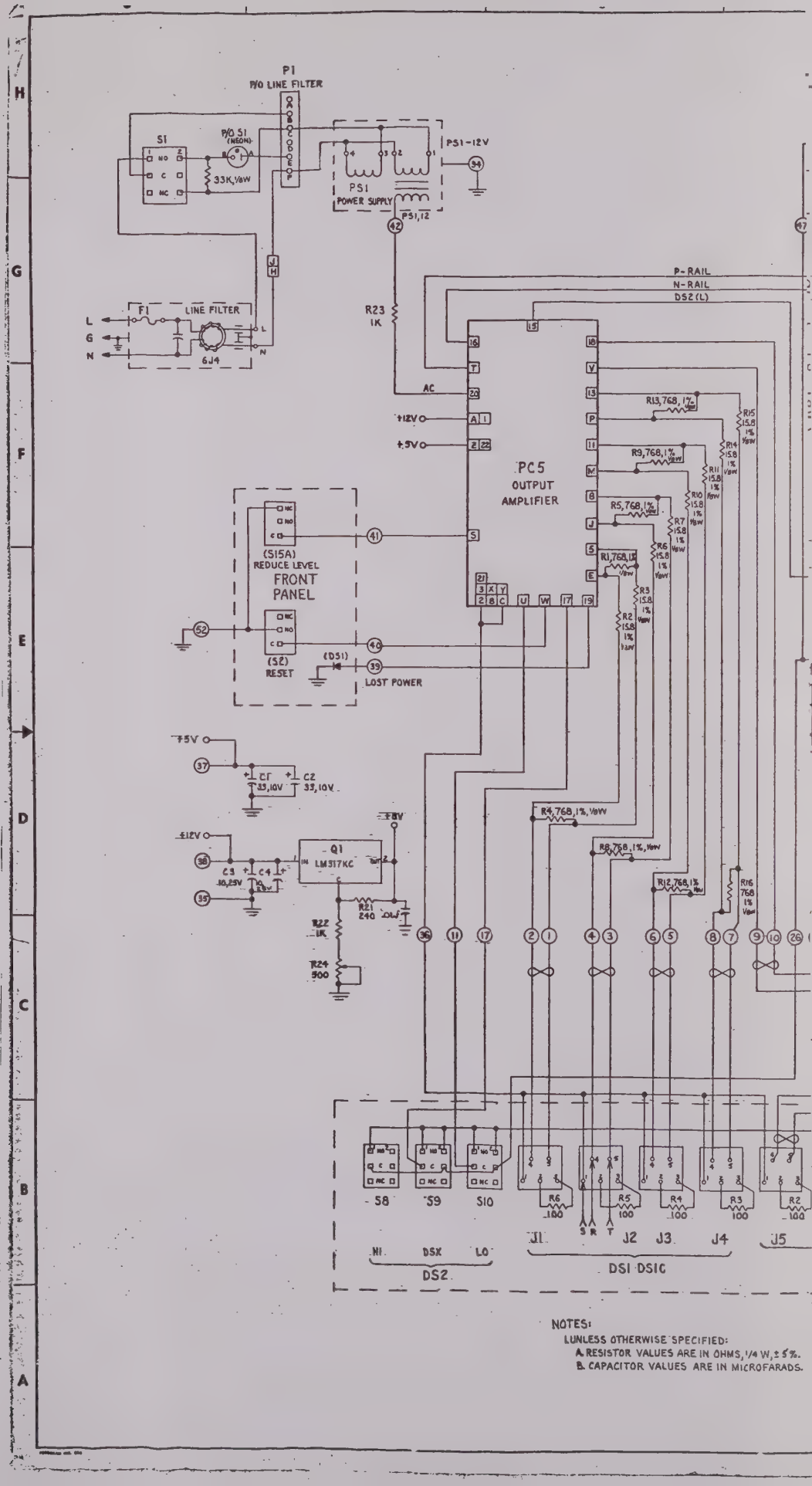
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE VALUES ARE IN OHMS. 1/8W ± 1%
   b. CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACES A PERMANENT REVISON LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA. TO BE COMPLETED BY TAU-TRON.

Fig. 6-6
1 of 3

ITEM	DESCRIPTION	PART NO.	QTY
3			
2	TX MOTHER PCB	9601-7125	1
1	CONNECTOR	9313-0001	4

L. FRANEK	11-26-79	TX MOTHER BOARD ASSY.	
R.A.L	11-28-79		
WEL	28-81		
		D-17126	H
		2-1 SS102	

D-17126



NOTES:
LUNLESS OTHERWISE SPECIFIED:
A. RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 5%.
B. CAPACITOR VALUES ARE IN MICROFARADS.

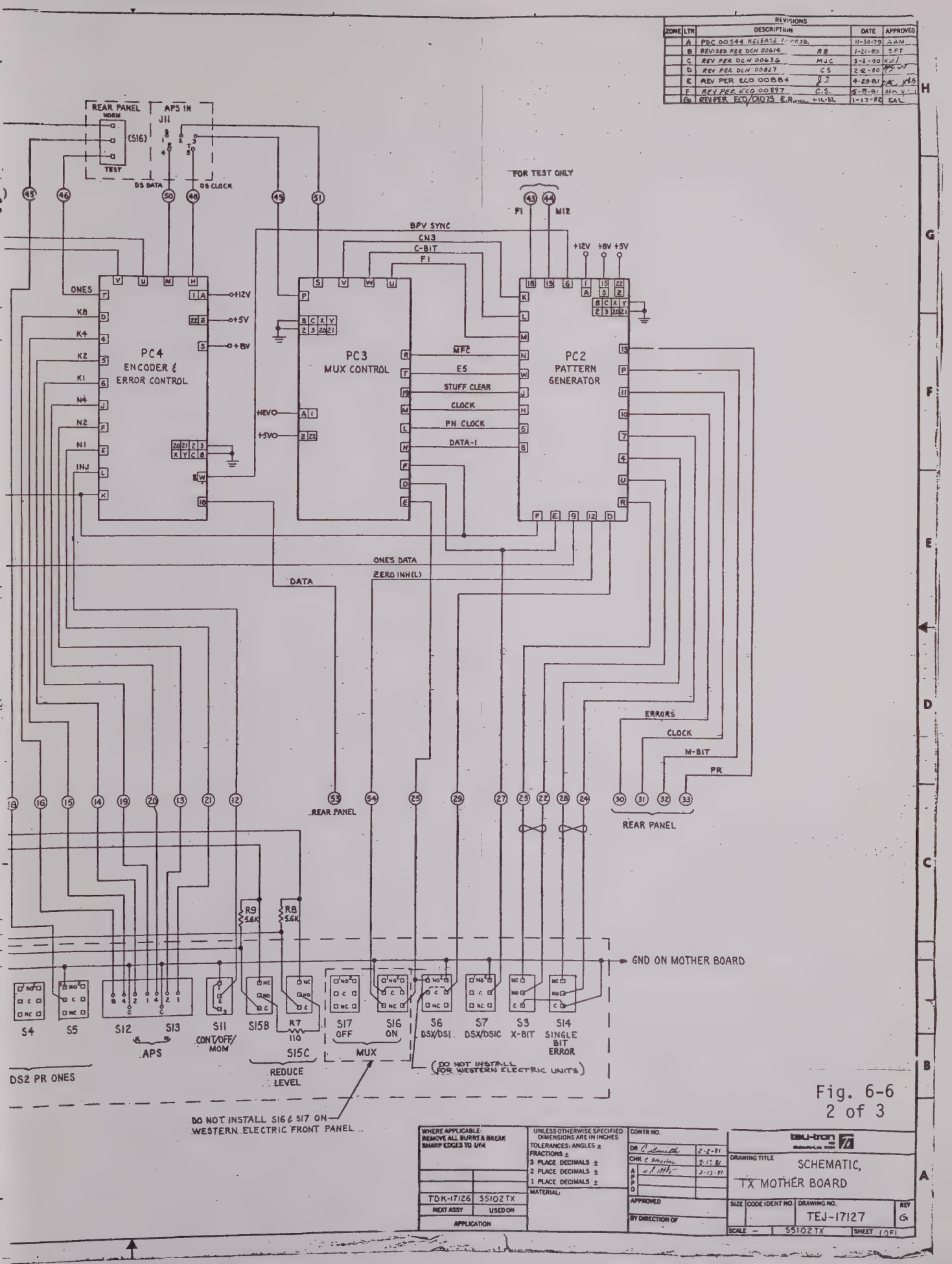
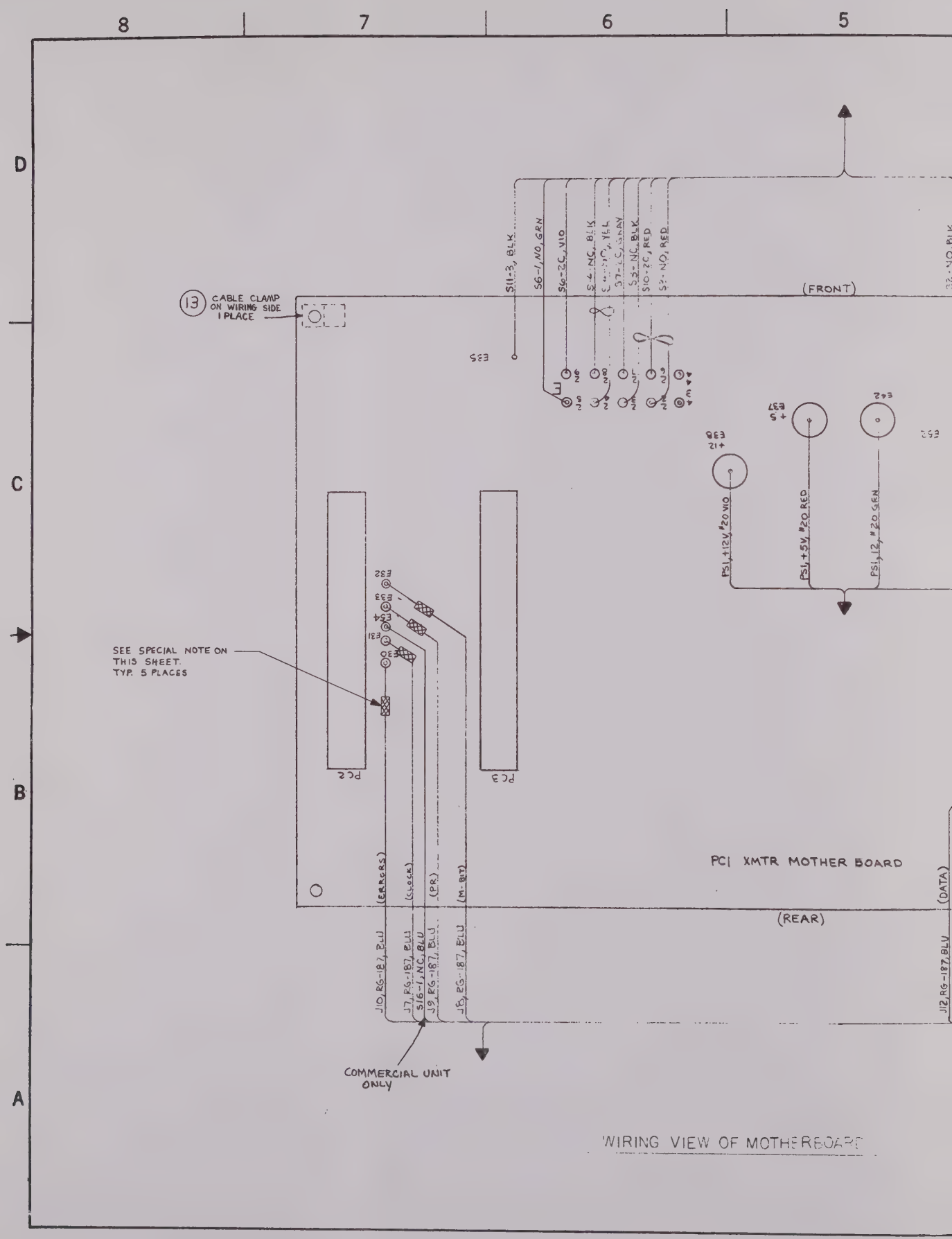
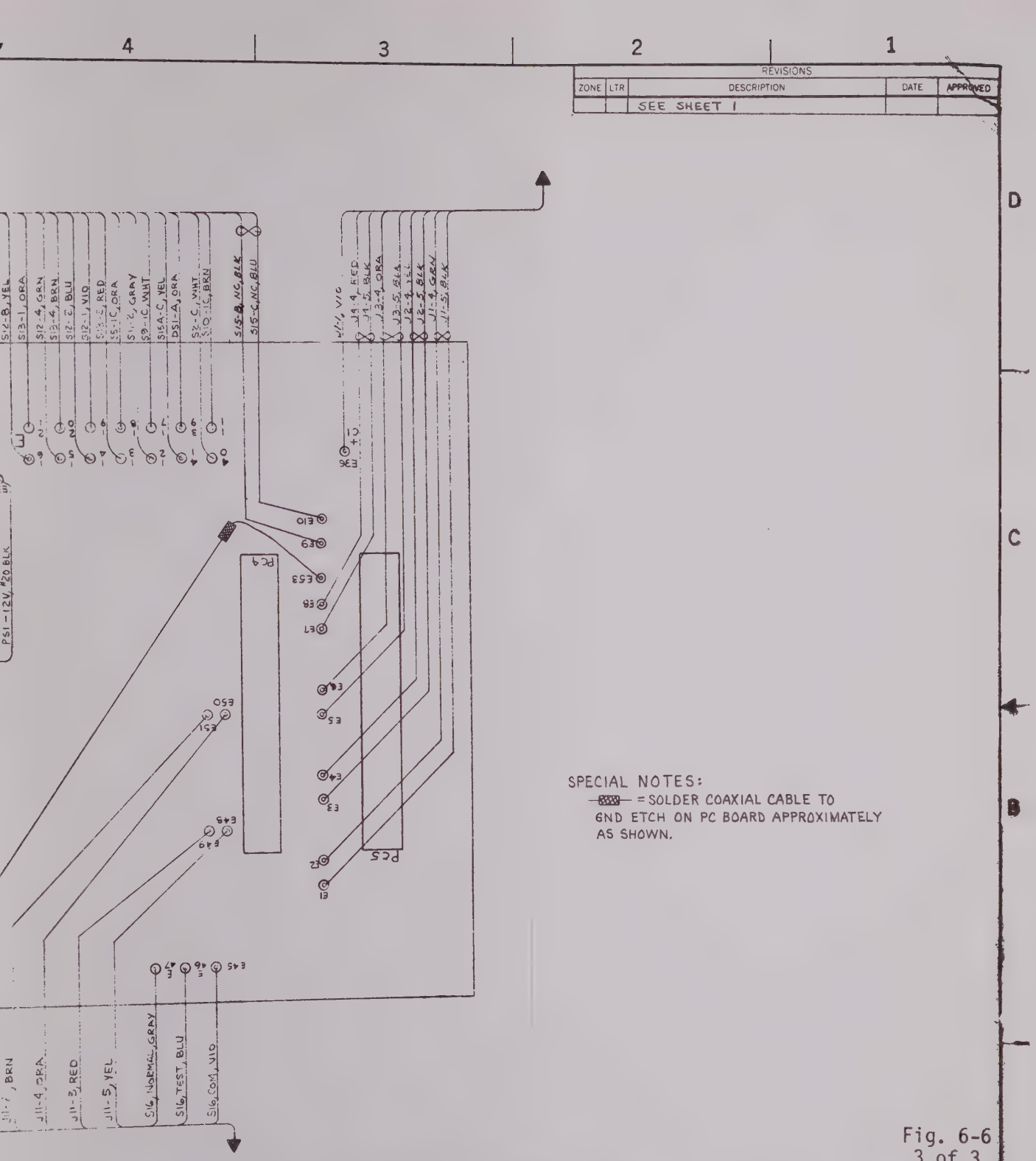

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A PDC 00544 RELEASE 11-30-79 AAM
B REVISED PER DCN 00614 RB 1-21-80 SFT
C REV PER DCN 00636 MJC 3-3-80
D REV PER DCN 00827 CS 2-12-80
E REV PER ECO 00884 4-29-81
F REV PER ECO 00897 C.S. 5-8-81
G REVISED PER ECO 01079 1-17-82 EAC
REAR PANEL
NORM
TEST
APS IN
J11
(S16)
DS DATA
DS CLOCK
FOR TEST ONLY
F1
M12
BPV SYNC
CN3
C-BIT
F1
+12V +8V +5V
PC4
ENCODER & ERROR CONTROL
PC3
MUX CONTROL
PC2
PATTERN GENERATOR
ONES
K8
K4
K2
K1
N4
N2
N1
INJ
+12V
+5V
+8V
+12VO
+5VO
MFC
ES
STUFF CLEAR
CLOCK
PN CLOCK
DATA-1
ONES DATA
ZERO INH(L)
DATA
ERRORS
CLOCK
M-BIT
PR
REAR PANEL
REAR PANEL
R9 5.6K
R8 5.6K
GND ON MOTHER BOARD
S4
S5
S12
S13
APS
S11
CONT/OFF/MOM
S15B
R7 110
S15C
REDUCE LEVEL
S17 OFF
S16 ON
MUX
S6 DSX/DS1
S7 DSX/DS1C
S3 X-BIT
S14 SINGLE BIT ERROR
(DO NOT INSTALL FOR WESTERN ELECTRIC UNITS)
DS2 PR ONES
DO NOT INSTALL S16 & S17 ON WESTERN ELECTRIC FRONT PANEL
WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:
CONTR NO.
DR C. Smith 2-2-81
CHK C. Smith 2-12-81
APPD 2-13-81
APPROVED
BY DIRECTION OF
TDK-17126 S5102TX
NEXT ASSY USED ON
APPLICATION
tau-tron
DRAWING TITLE
SCHEMATIC, TX MOTHER BOARD
SIZE CODE IDENT NO. DRAWING NO. REV
TEJ-17127 G
SCALE — S5102TX SHEET 1 OF 1

Fig. 6-6
2 of 3



WIRING VIEW OF MOTHERBOARD

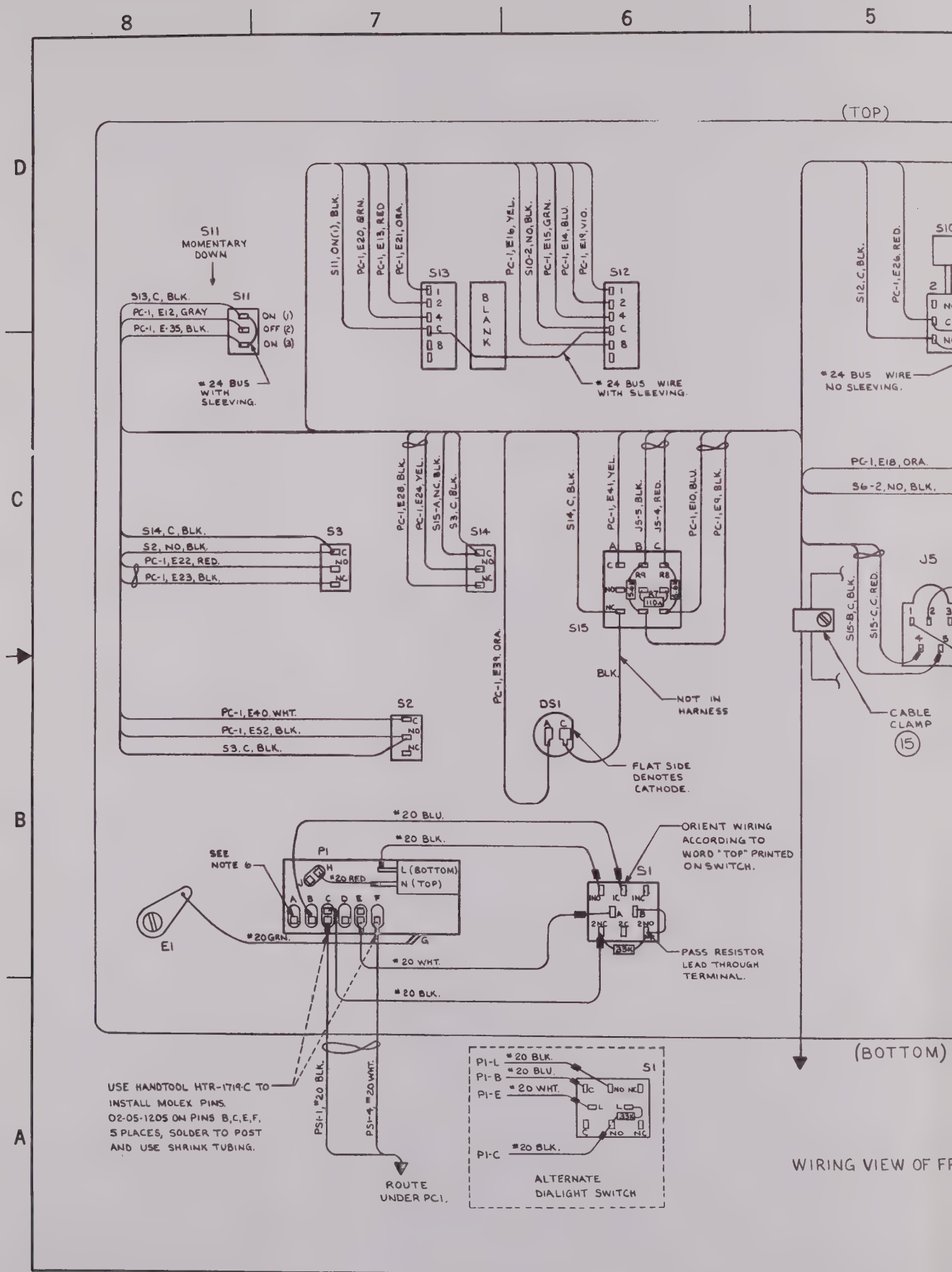


SPECIAL NOTES:

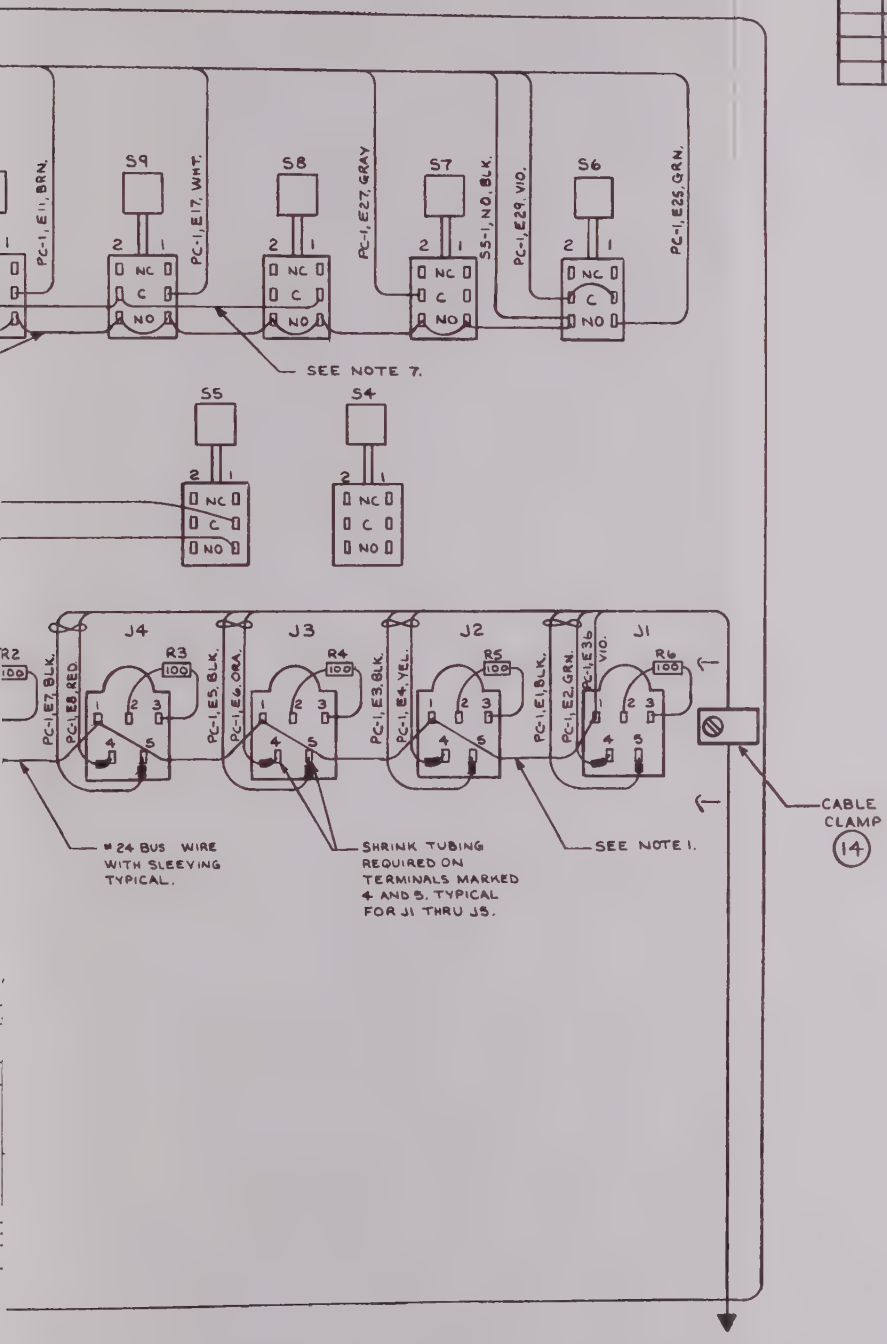
—▨— = SOLDER COAXIAL CABLE TO GND ETCH ON PC BOARD APPROXIMATELY AS SHOWN.

Fig. 6-6
3 of 3

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.: DR C. Smith 1-28-81 CHK BAC 2-12-81 APPD Wed Little 2-13-81 APPROVED BY DIRECTION OF	tau-tron INC Chelmsford, Ma. 01824 DRAWING TITLE: S5102Tx MOTHERBOARD WIRING DIAGRAM SIZE D | CODE IDENT NO. | DRAWING NO. TDM-1724 1 | REV C SCALE | S5102 TX | SHEET 3 OF 4
NEXT ASSY: S5102 Tx USED ON APPLICATION			


8
7
6
5
D
C
B
A
(TOP)
(BOTTOM)
S11
MOMENTARY
DOWN
S13, C, BLK.
PC-1, E12, GRAY
PC-1, E-35, BLK.
ON (1)
OFF (2)
ON (3)
#24 BUS WITH SLEEVING.
S11, ON(1), BLK.
PC-1, E20, BRN.
PC-1, E13, RED
PC-1, E21, ORA.
S13
S12
PC-1, E16, YEL.
S10-2, NO, BLK.
PC-1, E15, GRN.
PC-1, E14, BLU.
PC-1, E19, VIO.
#24 BUS WIRE WITH SLEEVING.
S12, C, BLK.
PC-1, E26, RED.
#24 BUS WIRE NO SLEEVING.
PC-1, E18, ORA.
S6-2, NO, BLK.
S14, C, BLK.
S2, NO, BLK.
PC-1, E22, RED.
PC-1, E23, BLK.
S3
PC-1, E28, BLK.
PC-1, E24, YEL.
S15-A, NC, BLK.
S3, C, BLK.
S14
S14, C, BLK.
PC-1, E41, YEL.
J5-5, BLK.
J5-4, RED.
PC-1, E10, BLU.
PC-1, E9, BLK.
S15
J5
S15-B, C, BLK.
S15-C, C, RED.
PC-1, E39, ORA.
BLK.
NOT IN HARNESS
CABLE CLAMP
15
PC-1, E40, WHT.
PC-1, E52, BLK.
S3, C, BLK.
S2
DS1
FLAT SIDE DENOTES CATHODE.
#20 BLU.
#20 BLK.
SEE NOTE 6
P1
#20 RED
L (BOTTOM)
N (TOP)
E1
#20 GRN.
S1
ORIENT WIRING ACCORDING TO WORD "TOP" PRINTED ON SWITCH.
PASS RESISTOR LEAD THROUGH TERMINAL.
#20 WHT.
#20 BLK.
USE HANDTOOL HTR-1719-C TO INSTALL MOLEX PINS. 02-05-1205 ON PINS B, C, E, F, 5 PLACES, SOLDER TO POST AND USE SHRINK TUBING.
P1-1, #20 BLK.
P1-4, #20 WHT.
ROUTE UNDER PC1.
P1-L
P1-B
P1-E
P1-C
#20 BLK.
#20 BLU.
#20 WHT.
#20 BLK.
S1
ALTERNATE DIALIGHT SWITCH
WIRING VIEW OF FR

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	0	ORIGINATED PER ECO 00897 CS	5-11-81	AAM 5-24-81
	1	ADDED JUMPER S6-2 TO S6-1C RN	8-20-81	BAC
	A	ADDED SHT. 1.	2-2-82	AAM
	B	FROM TDM-17245		
	C	REV PER ECO 01156 RN	7-19-82	RL AAM.



NOTES:

1. DRAPE THIS WIRE SO PC-4 CAN BE PLACED BETWEEN J1 AND J2.
2. ▬ DENOTES SHRINK TUBING REQUIRED.
3. RESISTORS ARE 1/8 WATT UNLESS SPECIFIED.
4. WIRES ARE TO BE #26 AWG UNLESS SPECIFIED.
5. ∞ DENOTES TWISTED PAIR #28 AWG.
6. ALL UNUSED PINS ON P1 MUST BE CUT OFF AFTER WIRING, (PINS A, D, E & J).
7. #24 BUS WIRE WITH SLEEVING UNLESS SPECIFIED.

Fig. 6-7
1 of 1

)NT PANEL.

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

	S5102 TX
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

CONTR NO.

DR C. SMITH	5-11-81
CHK A. MONTERIO	5-29-81
APPD	

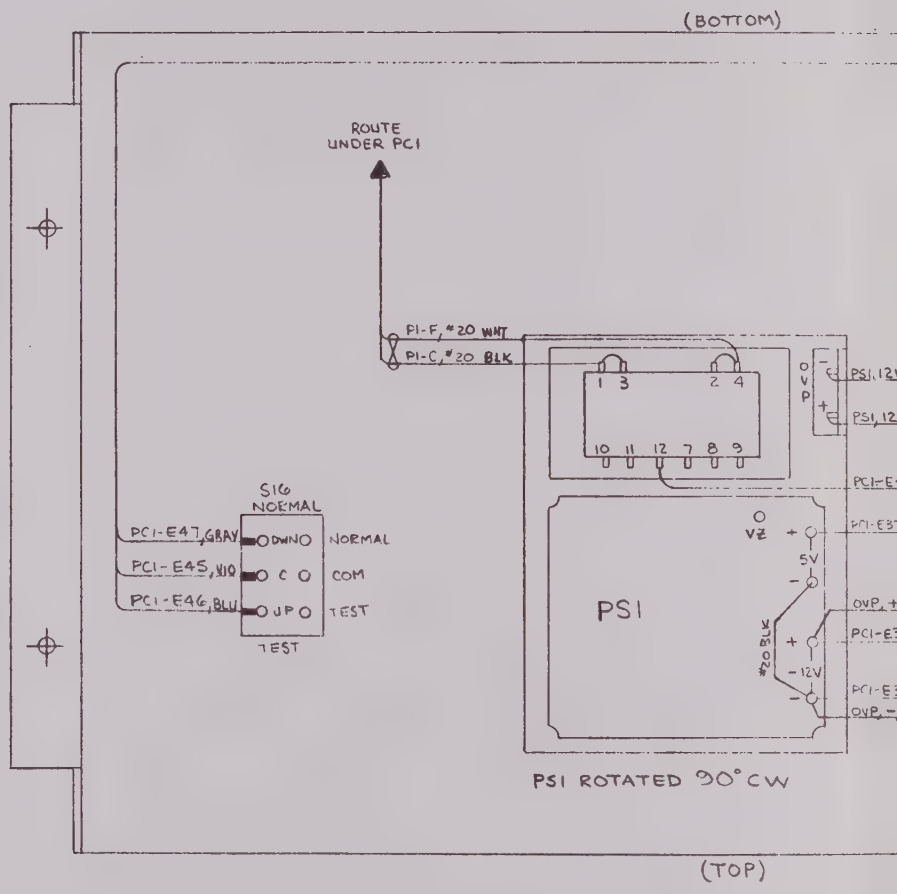
APPROVED
BY DIRECTION OF

tau-tron inc Chelmsford, Mass. 01824

DRAWING TITLE
(WESTERN ELECTRIC UNIT)
FRONT PANEL WIRING DIAGRAM.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		D-17241	C

SCALE — | S5102 Tx | SHEET 1 OF 4



CHASSIS WIRING VIEW

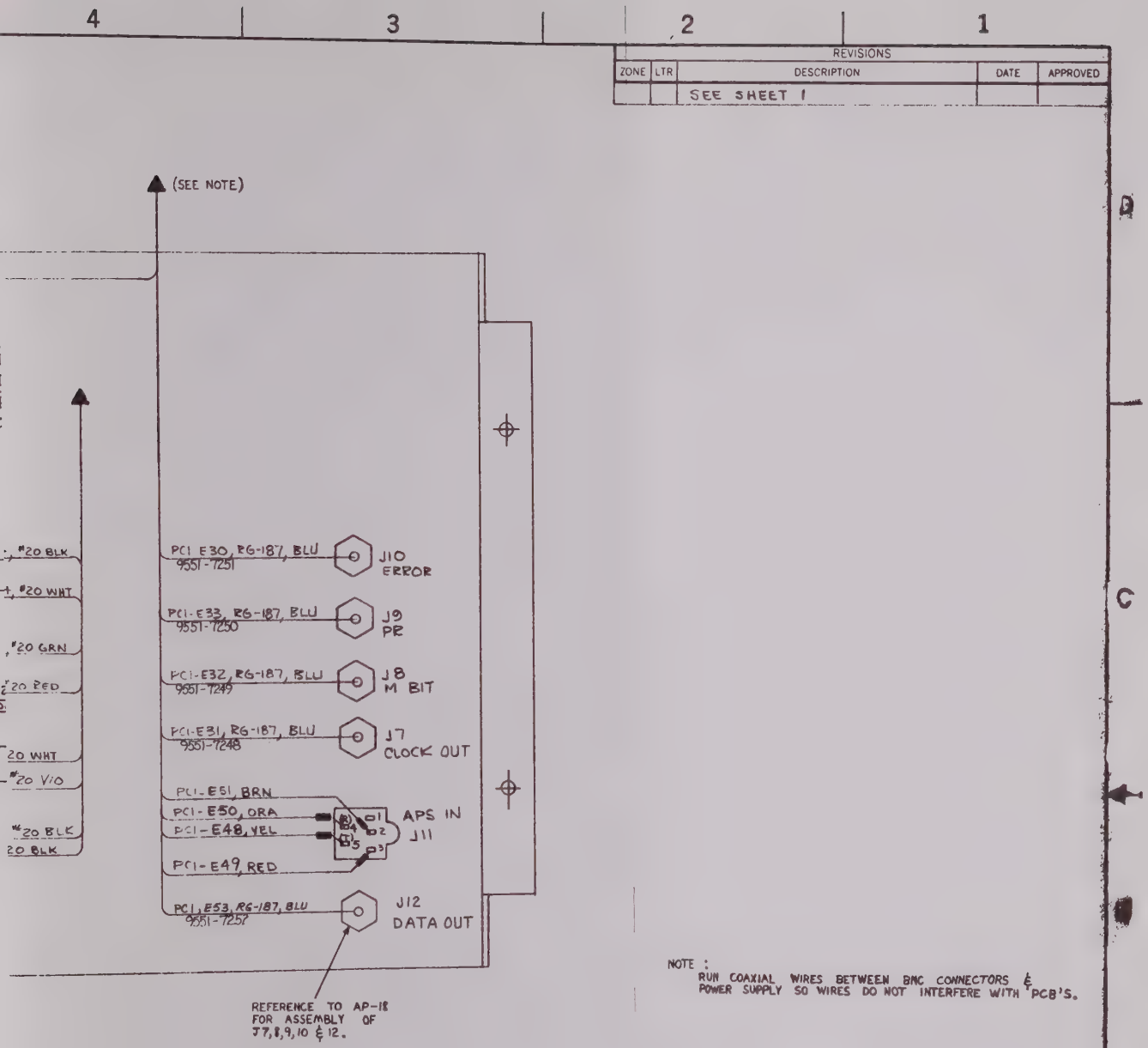


Fig. 6-8
1 of 1

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.	tau-tron INC Chelmsford, Mass. 01824	
		DR C. Smith 1-28-81	DRAWING TITLE	
		CHK B.A.C. 2-12-81	S5102 TX CHASSIS WIRING DIAGRAM	
		APPD		
S5102 Tx		APPROVED	SIZE: D	CODE IDENT NO.
NEXT ASSY / USED ON		BY DIRECTION OF	DRAWING NO.: TDM-17241	REV: C
APPLICATION			SCALE	S5102 TX

POWER-ONE INC.
D.C. POWER SUPPLIES

APPLICATION DATA
INCLUDING:

1. Schematic
2. Parts List
3. Specification
4. Outline & Mounting Drawing
5. General User Information

MODEL

OVP-12
OVP-24

SPECIFICATIONS:

Voltage Adjustment Range: 6.4 - 33 VDC

Maximum Current Rating		
Model	Intermittent	Continuous
OVP-12	12A	8A
OVP-24	30A	20A

Adjustment Procedure: (Note - Suggested OVP trigger voltages per Fig. A)

1. Connect Test circuit as shown in Fig. B. Test voltage source may be any power supply with a short circuit current limit of less than 8 amps (OVP-12) or 20 amps (OVP-24)
2. Energize and adjust the test voltage source to the desired OVP voltage.
3. Rotate the OVP adjustment pot CCW (from its maximum CW position) until the OVP fires as indicated by a 1V reading on M1. Leave the pot in this position, unit is now ready for installation into power supply.
4. Bolt the OVP onto the power supply using the mounting holes provided. Connect the white (+) lead to the positive output and the black (-) lead to the negative output.

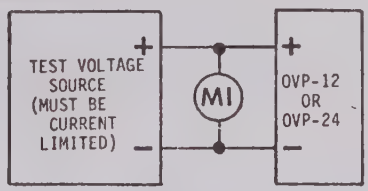


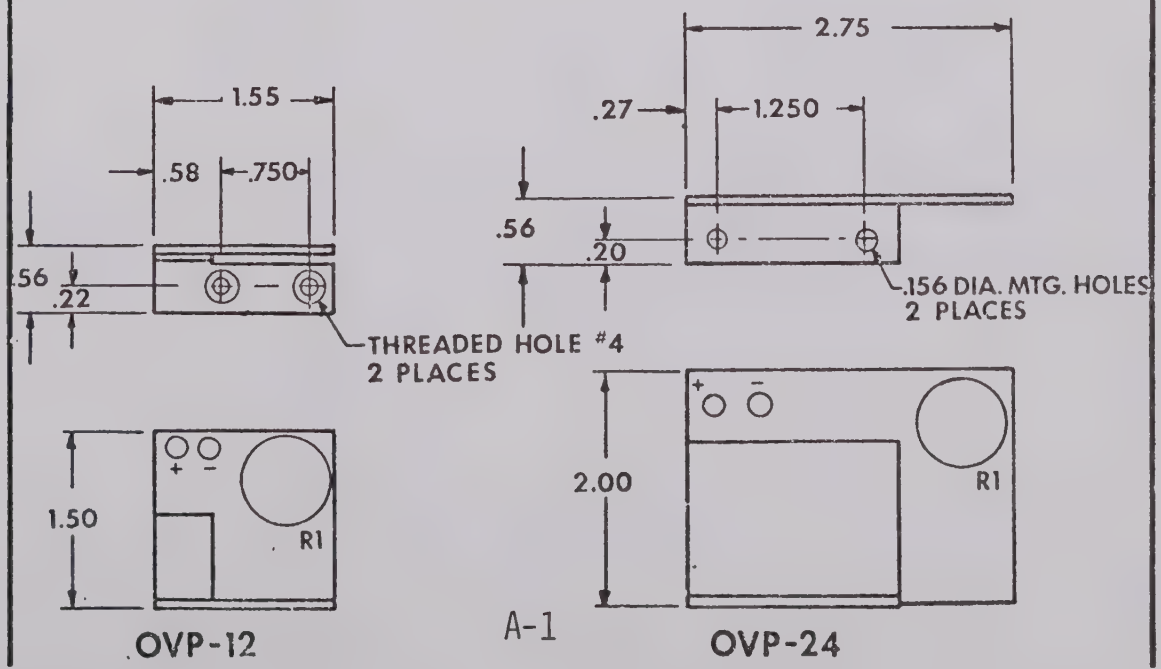
Figure B

Power Supply Output Voltage	Suggested OVP Trigger Voltage
5 6 12	6.4+.4 7 14
15 18 20	17 21 23
24 Dual +12 Dual ±15	27 27 33

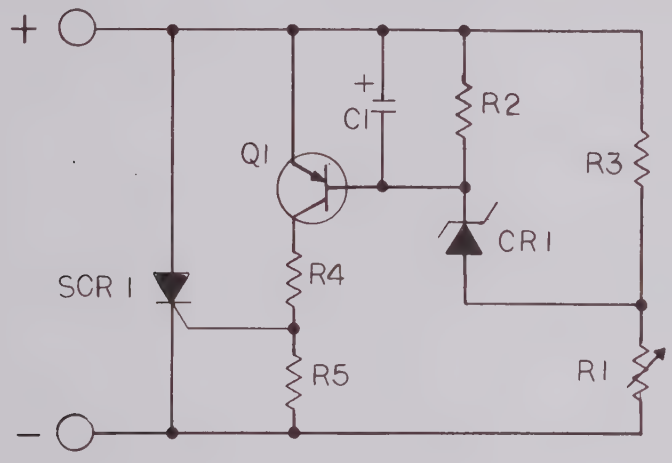
Figure A

2 YEAR GUARANTEE

POWER-ONE will repair any power supply of its manufacture that does not perform to published specifications as a result of defective materials or workmanship for a period of 2 years from date of original purchase. No other obligations or liabilities are implied or expressed. Returns must be freight prepaid.



REF DES	OVP 12	STD P/N	DESCRIPTION
BRACKET	11151	412-11151	BRACKET
C1	1/50V	101-10111	CAPACITOR ALUM.ELECT.
CR1	IN752A	112-10006	DIODE, ZENER
R5	330Ω	151-10353	RESISTOR ½W 5% CF
R4	47Ω	151-10333	
R2	1K	151-10365	
R3	270Ω	151-10351	RESISTOR ½W 5% CF
R1	1.5K	155-10085	POTENTIOMETER 2W, WW
SCR1	S0508LS3	160-10013	SCR
Q1	2N2907A	172-10248	TRANSISTOR
PCB	11150	505-11150	PRINTED CIRCUIT BOARD



OVP-12

TROUBLESHOOTING GUIDE	
SYMPTOM	POSSIBLE PROBLEM
UNIT STAYS ON (SHORTED) AFTER AN OVERVOLTAGE CONDITION IS CORRECTED	SCR 1 SHORTED Q1 SHORTED CR1 SHORTED
RESISTANCE CHECK INDICATES UNIT SHORTED	SCR 1 SHORTED
ERRATIC TRIGGERING OR NOISE SPIKES OR TRANSIENTS	C1 OPEN
UNIT WILL NOT TRIGGER	SCR 1 OPEN Q1 OPEN CR1 OPEN C1 OPEN R4 OPEN

Repair Returns

To return a unit for repair:

1. Call the Customer Service Dept., **(617) 256-9013**, for a **Repair Authorization Number.** This will reduce administrative delays and ensure prompt return of your unit.
2. Complete and **attach one of the Repair Tags** below to your unit.
3. **Pack the unit** in the original shipping carton and packaging materials, if available. Otherwise use a double-walled carton (test strength of 350 lb) and shock absorbing material such as bubble wrap to prevent the unit from moving in the carton during transit. Seal with heavy paper tape.
4. **Send to:**

   Tau-Tron
   27 Industrial Ave.
   Chelmsford, MA 01824
   atten: Customer Service

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0163-1181A

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Feedback

Your Feedback is Important

In fact it's necessary to help us produce an instruction manual that meets your needs. If you have any suggestions, corrections, or questions, we'd like to hear from you.

If you have any feedback, please complete, detach, and mail the lower card

If you would like a representative to call, require additional information, or would like to be placed on our mail list to receive **The Pulse** or other useful technical information, please complete, detach, and mail the card below.

Please —

☐ Have representative call.

☐ Add me to your mail list.

Send additional information on:

☐ Bit Error Rate Test Equipment
☐ Data/Word Generators
☐ Data Loggers
☐ High-Speed Components

My general application is _____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State & Zip _____ Phone _____

Instruction Manual Form Number ☐☐☐☐–☐☐☐☐☐

Comments _____

_____

_____

from:

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State & Zip _____ Phone _____

Form 0159A-0183C

Tau-tron Inc. 27 Industrial Ave., Chelmsford, MA 01824